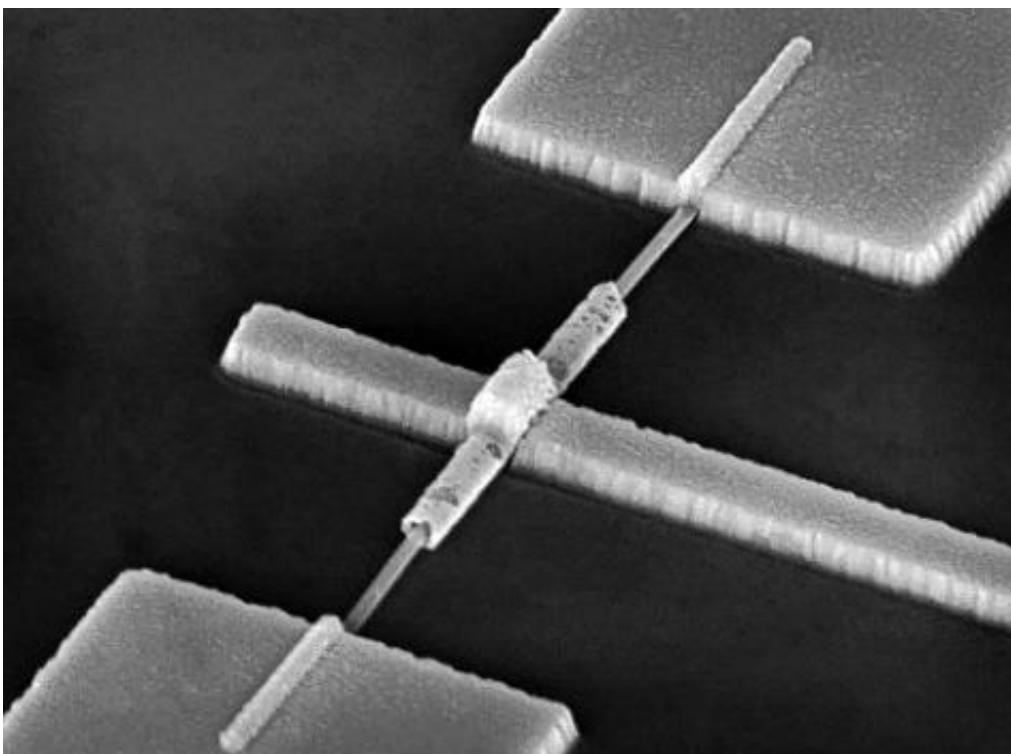


It's a wrap! Nanowire opens gate to new devices

April 7 2011, By Bob Beale



A scanning electron micrograph of the horizontal wrap-gate nanowire transistor.
Image courtesy of Adam Micolich.

(PhysOrg.com) -- In an interesting feat of nanoscale engineering, researchers at Lund University in Sweden and the University of New South Wales have made the first nanowire transistor featuring a concentric metal 'wrap-gate' that sits horizontally on a silicon substrate.

Two remarkable aspects of their design are the simplicity of the fabrication and the unique ability to tune the length of the wrap-gate via a single wet-etch step, notes Associate Professor Adam Micolich, an ARC Future Fellow in the Nanoelectronics Group in the UNSW School of Physics.

Packing ever higher densities of transistors into a [microchip](#) comes at a hefty price – the reduced overlap between the semiconductor channel through which the current flows and the metal gate makes it harder to switch the current on and off.

This drove the development of the ‘Fin Field-Effect Transistor’, or FinFET, where the silicon either side of the channel is etched away to create a raised mesa structure. This allows the gate to fold down around the sides of the channel, improving the switching without increasing the chip space needed by the device. Even better control can be obtained by wrapping the gate all the way around the channel. But getting metal underneath the channel without compromising the device can be a formidable task using conventional ‘top-down’ silicon microfabrication techniques.

This has led to significant interest in self-assembled [nanowires](#) for computing applications (see D.K. Ferry, [doi: 10.1126/science.1154446](https://doi.org/10.1126/science.1154446)). These tiny semiconductor needles, around 50 nm in diameter and up to several microns in length, are grown using chemical vapour deposition and stand vertically on a semiconductor substrate, making it possible to deposit an insulator and gate metal around the nanowire’s entire outer surface.

Although these coated nanowires can be made into fully-functioning transistors in the vertical orientation, the process to achieve this is very involved. And in many cases, it is more desirable to have the nanowire transistor lying flat on the substrate, as with conventional silicon

transistors. This poses an interesting challenge for nanotechnologists: Is it possible to make nanowire transistors with an all-around metal ‘wrap-gate’ that lay flat on a semiconductor substrate?

In work published this week in *Nano Letters* [Storm *et al.* [doi:10.1021/nl104403g](https://doi.org/10.1021/nl104403g)], the team not only demonstrate the first such horizontal wrap-gate nanowire transistors, but they demonstrate that they can be made using a remarkably simple process that allows them to precisely set the wrap-gate’s length using a single wet-etch step, without any need for further lithography.

Their approach exploits the etchant solution’s ability to undercut the resist and etch along the nanowire, producing gates that range in length from slightly less than the contact separation to as low as 100 nm, simply by tuning the etchant concentration. The resulting devices have excellent electrical performance and can be produced reliably with high yield.

Beyond being a significant advance in nanofabrication techniques, these devices open interesting new avenues for fundamental research.

The wrap-gated nanowires are ideal for studies of one-dimensional quantum transport in semiconductors, where remarkable phenomena such as electron crystallization and spin-charge separation may be observed. Additionally, the strong gate-channel coupling combined with an exposed gold wrap-gate surface offers interesting potential for sensing applications by utilising the established chemistry for binding antibodies and other polypeptides to gold surfaces.

Provided by University of New South Wales

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