

Samsung releases 1-Gbit DRAM chip with 512-pin wide I/O interface

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(PhysOrg.com) -- Samsung Electronics announced the development of a 1-Gbit DRAM chip. It features a 512-pin wide I/O interface that is designed for a variety of mobile applications including smartphones and tablet PC's.

In order to boost the data transmission the chip uses 512 pins for the data input and output. When we compare this to the previous generation of mobile DRAMs, which used a maximum of 32 pins, we can see that a significant improvement in the [processing power](#) of [mobile devices](#) is expected.

In case you do not have an active imagination the I/O 1-Gbit WIO DRAM can transmit data at a rate of 12.8-Gbytes per second, while reducing the [power consumption](#) by approximately 87 percent. The bandwidth that this chip is expected to handle is estimated be about four times that of LPDDR2 DRAM, which runs at approximately 3.2-Gigabytes per second according to Samsung. If you include the pins for the commands, the power supply and its regulation the WIO DRAM, it is designed to have ip to 1,200 pins.

Samsung was a bit sketchy on the details, with no indications give as to whether or when the company intends to offer the 1-Gbit WIO DRAM as a packaged part or for commercial use or as part of a bare die in multi-chip packages. They were also not giving a great deal of information about when engineering samples of the 1-Gbit WIO DRAM would be made available or when the chip will be in volume production for use in

devices.

As a follow up to this WIO DRAM launch Samsung has released plans for a 20-nm class 4-Gbit WIO mobile DRAM which will become available at some point in 2013.

More information: Samsung PR: [www.samsung.com/global/business... View.do?news_id=1236](http://www.samsung.com/global/business...View.do?news_id=1236)

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