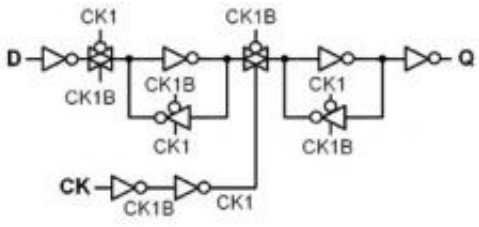
New energy-saving flip-flop circuit developed by Toshiba

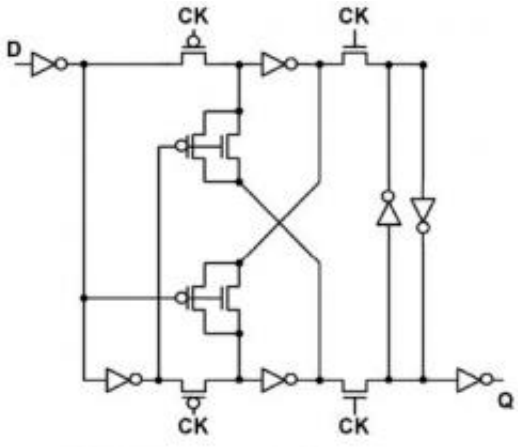
February 21 2011



Conventional circuit configuration.

Toshiba Corporation today announced that it has developed a new flip-flop circuit using 40nm CMOS process that will reduce power consumption in mobile equipment. Measured data verifies that the power dissipation of the new flip-flop is up to 77% less than that of a typical conventional flip-flop and that it achieves a 24% reduction in total power consumption when applied to a wireless LAN chip.

A flip-flop is a circuit that temporarily stores one bit of data during arithmetic processing by a digital system-on-a-chip (SoC) incorporated in mobile equipment and other digital equipment. As a typical SoC uses 100,000 to 10 million flip-flops they are an essential part of an SoC design.



Circuit configuration of new technique.

A typical flip-flop incorporates a clock buffer to produce a clock inverted signal required for the circuit's operation. When triggered by a signal from the clock, the clock buffer consumes power, even when the data is unchanged. In order to reduce this power dissipation, a power-saving design technique called clock gating is widely used to cut delivery of the clock signal to unused blocks. However, after applying the clock gating, the flip-flop active rate, a measure of data change rate per clock, is only 5-15%, indicating that there is still plenty of room for further power reduction.

In order to save power, Toshiba changed the structure of the typical flip-flop and eliminated the power-consuming clock buffer. This approach brings with it the problem of data collision between the data writing circuitry and the state holding circuitry in the flip-flop, which Toshiba overcame by adding adaptive coupling circuitry to the flip-flop. A combination of an nMOS transistor and a pMOS transistor, this circuitry adaptively weakens state-retention coupling and prevents collisions. Despite the addition of the adaptive coupling circuitry, overall simplification of the basic flip-flop configuration reduces the transistor

count from 24 to 22, and the cell area is less than that of the conventional flip-flop.

This achievement will be announced on February 23 (local time) at the 2011 IEEE International Solid-State Circuits Conference (ISSCC) now being held in the United States.

Provided by Toshiba Corporation