

Researchers develop a full numerical model of EUV imaging and exposure statistics

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The tolerances on feature size, shape, and placement for next generation computer chips fabricated with extreme ultra-violet (EUV) lithography will range from a maximum of a few nanometers down to less than 1 nm.

To achieve these tolerances, the sidewall [roughness](#) of the features, traditionally called line edge roughness (LER), is required to be less than 2 nm.

The CNST's Gregg Gallatin and Lawrence Berkley National Laboratory's Patrick Naulleau have developed a numerical model* that accounts for the two dominant sources of LER: the quantum statistics of exposing and developing the resist; and the roughness of the mask features themselves.

Mask LER is about 10 nm, which reduces to 2 nm on the [wafer](#) using a 5X EUV imaging system.

The model determines the relative contribution each LER source makes to the wafer under various imaging and processing conditions. It predicts wafer LER and also determines to what extent the frequency content of the mask contribution is altered by the imaging, exposure, and development processes.

The researchers have discovered that there are combinations of processes where the mask induced roughness is the dominant contributor

to wafer LER, but its frequency signature is virtually indistinguishable from the contributions of exposure and development statistics alone.

Therefore, other direct metrology methods in addition to wafer LER frequency content will be required to determine the separate contributions. This work supports the continued progress of semiconductor manufacturing technology.

More information: *The Effect of Resist on the Transfer of Line-edge Roughness Spatial Metrics from Mask to Wafer, G. M. Gallatin and P. P. Naulieau, *Journal of Vacuum Science & Technology B*, 28, 1259-1266 (2010). [avspublications.org/jvstb/reso ...
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