UCLA receives grant for ongoing research on high-speed, high-density computer memory

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A team of researchers at UCLA's Henry Samueli School of Engineering and Applied Science has been awarded $5.5 million for ongoing efforts to develop technology they expect will lead to computers and other devices that use less power and require virtually no start-up time when turned on.

The grant from the Defense Advanced Research Projects Agency will fund continuing research on a potential universal memory — a high-speed, high-capacity computer memory that is compatible with current standards of design and manufacture in the computer and electronic device industries. The agency had previously awarded UCLA Engineering $5 million for the first phase of this research program.

The researchers, led by Kang Wang, UCLA's Raytheon Professor of Electrical Engineering, are working on a memory technology known as spin-transfer torque magnetoresistive random access memory (STT-RAM), which has great potential over other types of memory currently in use.

STT-RAM can achieve a density comparable to dynamic random access memory (DRAM), the most common type of main memory for personal computers, allowing for extremely small chips. And it equals — and has even exceeded — the high speed of static random access memory (SRAM), which is often used for caches in computer microprocessors. Both types of memory keep programs running fast. And like the flash memory common in USB drives and memory cards, STT-RAM retains

its memory without any power while being orders of magnitude faster and more energy efficient.

STT-RAM could combine these three advantages into a single scalable memory technology with excellent endurance and very low power requirements, researchers say. And it could be implemented across a range of devices, including personal computers and mobile communication devices.

"STT-RAM is a non-volatile memory technology with great promise," Wang said. "It will facilitate low-power, high-speed applications. More importantly, it may become a completely new platform of non-volatile electronics when integrated with today's complementary metal-oxide semiconductor (CMOS) circuits. This new platform will have no standby power dissipation and require no turn-on time for many mobile applications."

The UCLA Engineering research team completed the first phase of the project a year early by meeting challenging requirements on the speed, energy consumption and stability of STT-RAM magnetic bits through a series of material and structure innovations.

In this newly funded second phase, the group will further improve the energy and stability metrics and build prototype chips to demonstrate how STT-RAM can be implemented with CMOS read/write circuits.

"The device performance that we needed to achieve in order to meet the goals of the first phase was very challenging," said Pedram Khalili, a research associate at UCLA and the project's manager. "This included write times smaller than 5 nanoseconds and write energies lower than 0.25 picojoules per bit. We not only met but in fact significantly surpassed these metrics due to a great team effort.

"An important emphasis of the second phase, in addition to further improving the device performance metrics, will be statistical studies needed to facilitate integration with CMOS to realize a product," he said.

The spin-transfer torque (STT) effect is a recent discovery that exploits the natural spin of electrons to electrically change the magnetic orientation of a material. During STT switching, a spin-polarized current is used to exert a force on a magnetic layer, resulting in the layer switching its relative orientation.

The key to making STT-RAM work is the use of magnetic tunneling junctions, sandwiches of two magnetic materials with a thin insulating tunneling barrier between them. The technology is "non-volatile," meaning the magnetic layers do not require power to retain memory.

Thanks to its efficient spin-transfer torque techniques, the STT-RAM technology developed at UCLA has another major benefit: a low writing current, on the order of 100 microamperes or less for semiconductors at the standard 45- and 65-nanometer nodes. With future semiconductor nodes, writing current will continue to scale down significantly. This lower current translates to a denser, less-expensive memory.

In addition, while STT-RAM speed can be equivalent to SRAM, the UCLA Engineering researchers have made innovations in materials and structure for STT-RAM. This has produced writing speeds for an individual cell in STT-RAM ranging down to 100 picoseconds, which is an order of magnitude faster than current SRAM speeds.

Provided by University of California - Los Angeles

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