Imec reports progress in deep sub-micron scaling for logic and memory

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At the International Electron Devices Meeting in San Francisco Imec's advanced CMOS research program reports promising advances in scaling logic, DRAM and non-volatile memory.

A new device based on non-silicon channels was realized to scale high-performance logic towards the sub-20nm node. Moreover, Imec developed low-leakage capacitors allowing DRAM to be pushed to the 2x nm node. And the switching mechanism of resistive RAM for next-generation flash memories (RRAM) has been unraveled.

Implant-free SiGe channels to scale logic ICs towards the sub-20nm node

Further scaling of CMOS towards the sub-20nm node requires higher mobility channels and novel device structures to boost transistor performance. Imec developed a new implant-free SiGe (silicon germanium) quantum well pFET device featuring a high-mobility SiGe channel with raised SiGe source/drains using bulk-Si substrates. This high-electron mobility transistor with an EOT (effective oxide thickness) of 0.85 achieves a 50% higher saturation drive current compared to Si-controlled pFETs. The device concept is compatible with additional strain boosters paving the way to deep-submicron scaling achieving high performance.

Low-leakage MIM (metal insulator metal) capacitors

enabling 2x nm node DRAM

Imec reports as the world first a viable path to scale DRAM to the 2x node by using novel stack engineering. To scale DRAM to the 2x nm node, low leakage at an EOT of 0.4nm and less is required, deposited with highly conformal atomic layer deposition (ALD) processes for compatibility with large aspect ratio structures. Up to now, this was indicated in red as "manufacturable solutions not known" by the international roadmap for semiconductors (ITRS). Imec today reports record low-leakage MIM capacitors, JG of 10^{-6} A/cm^2 at 0.4nm EOT, enabling to scale DRAM to the 2x nm node. The capacitors were realized using a novel TiN/RuOx/TiOx/STO/TiN stack fabricated in a 300mm line with DRAM compatible processes.

Fundamental understanding of switching mechanism of RRAM

RRAM is a promising alternative concept for future flash memory, indicated on the roadmap to be in production within 3 to 4 years. To realize a RRAM technology ready for mass production, fundamental understanding of the switching mechanism is required. The operation of RRAM relies on the voltage-controlled resistance change of a MIM capacitor. Many stacks of combinations of materials need a forming step to create a small conductive filament connecting the electrodes. In the reliability community, this is known as dielectric breakdown. RRAM operation is thus based on the repetitive opening and closing of a dielectric breakdown path. Imec applied its reliability knowledge of logic to RRAM, resulting in fundamental understanding of the switching mechanism of RRAM. By finding synergies between conventional logic ICs and RRAM, imec succeeded in setting out the theory for predicting the maximum applicable Vset and revealed that the reset operation corresponds to a pinch off of the filament at its narrowest point.

These results were obtained in cooperation with Imec's key partners in its core CMOS programs: Intel, Micron, Panasonic, Samsung, TSMC, Sony, Fujitsu, Infineon, Qualcomm, ST Microelectronic and Amkor.

Source: IMEC

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