

# Meeting consumers' HD demands with a faster algorithm

July 7 2010, by Kurt Pfitzer

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(PhysOrg.com) -- Engineers help smaller processors outperform a single superfast processor by working more efficiently in parallel.

In their insatiable demand for faster, smaller and more [mobile communications](#) gadgets, says Zhiyuan Yan, consumers are straining the capacity of information technology.

[Handheld devices](#) that offer high-definition (HD) images and portability—such as cell phones with cameras and Internet access—require high throughput, or processing speed, says Yan, an assistant professor of electrical and [computer engineering](#). To be portable and small, the devices must also be able to operate with little power.

These two trends—greater performance and stringent power requirements—pose challenges to the technology and the mathematical equations on which the IT revolution has relied.

“HD applications require high throughput and low power in order to be handheld and mobile,” says Yan. “When you take these two together, you’re in a sense burning the candle at both ends.”

Yan and Meghanad Wagh, an associate professor of electrical and computer engineering, recently received a three-year grant from the National Science Foundation to devise scalable bilinear algorithms to help meet these challenges.

“This project represents a different way of thinking about algorithms,” says Wagh. “Normally in signal processing, you write algorithms meant for standard computer architectures. But to achieve the required speed, we have developed an entirely new class of algorithms that can be directly cast into hardware. Our new algorithms are extremely fast and take advantage of the new trend in technology.”

## **Helping smaller processors work faster in parallel**

The new algorithms are more suitable than traditional algorithms for high-performance computing.

“The IT revolution of the last 20 years has been driven in part by the scaling of CMOS [complementary metal-oxide semiconductor] technology,” says Yan. “We can pack more information in smaller chips, but the more we do this, the closer we approach the limits of technology.”

“Until a few years ago, to improve computer speed, you used a larger processor. Now, you split the computation and do it in parallel with many smaller processors. Many less-powerful processors can be just as good as or better than one superfast processor, while consuming less power.

“The trouble is that a lot of traditional signal-processing algorithms are not parallelizable and therefore cannot take advantage of these new ideas.”

Parallel processing, say Yan and Wagh, allows separate applications of a multimedia system to be dedicated to specific processors. Video games might use one processor for graphics, a second for manipulating objects on the screen, and a third for the remaining system computations. This helps prevent overloading a single [processor](#) with competing demands.

“Our algorithms are inherently structured,” says Yan. “This enables us to extract the maximum parallelism in processing and to offload tasks to dedicated hardware.”

Another advantage of the Lehigh researchers’ algorithms is that they can be scaled to handle the greater level of complexity required by computationally intensive jobs.

### **“Scaling gracefully to handle size and complexity”**

“Our algorithms scale gracefully and deal easily with size and complexity,” says Yan. “The earlier algorithms worked fine for small problems, but problems have become more complex. Without algorithms like ours, this complexity would overwhelm processors.

“Our goal is to make it possible for information technologies to continue to improve at the rate that consumers are accustomed to.”

Wagh and Yan have published articles in the top journals of their field, including *IEEE Transactions on Signal Processing*, *IEEE Signal Process Letters*, and Elsevier’s [Signal Processing](#). One of Yan’s students and two of Wagh’s have earned Ph.D.s in this area.

Provided by Lehigh University

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