Aiming to boost electronics performance, researchers capture images of sub-nano pore structures for the first time

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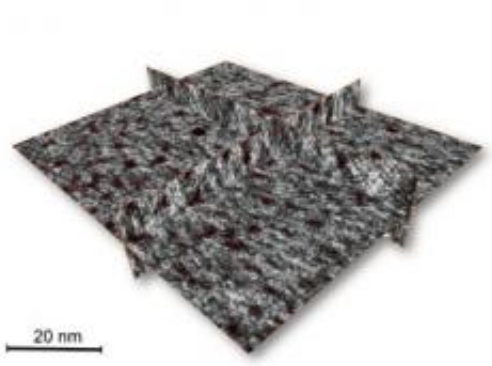

An image showing nanoscale pores in the dielectric material. (Huolin Xin/Muller Group)

(PhysOrg.com) -- Moore's law marches on: In the quest for faster and cheaper computers, scientists have imaged pore structures in insulation material at sub-nanometer scale for the first time. Understanding these structures could substantially enhance computer performance and power usage of integrated circuits, say Semiconductor Research Corporation (SRC) and Cornell University scientists.

To help maintain the ever-increasing power and performance benefits of semiconductors - like the speed and memory trend described in Moore's law - the industry has introduced very porous, low-dielectric constant

materials to replace silicon dioxide as the insulator between nano-scaled copper wires. This has sped up the electrical signals sent along these copper wires inside a computer chip, and at the same time reduced power consumption.

"Knowing how many of the molecule-sized voids in the carefully-engineered Swiss cheese survive in an actual device will greatly affect future designs of integrated circuits," said David Muller, Cornell University professor of applied and engineering physics, and co-director of Kavli Institute for Nanoscale Science at Cornell. "The techniques we developed look deeply, as well as in and around the structures, to give a much clearer picture so complex processing and integration issues can be addressed."

The scientists understand that the detailed structure and connectivity of these nanopores have profound control on the mechanical strength, chemical stability and reliability of these dielectrics. With today's announcement, researches now have a nearly atomic understanding of the three-dimensional pore structures of low-k materials required to solve these problems.

Welcome to the atomic world: SRC and Cornell researchers were able to devise a method to obtain 3-D images of the pores using electron tomography, leverages imaging advances used for CT scans and MRIs in the medical field, says Scott List, director of interconnect and packaging sciences at SRC, at Research Triangle Park, N.C. "Sophisticated software extracts 3-D images from a series of 2-D images taken at multiple angles. A 2-D picture is worth a thousand words, but a 3-D image at near atomic resolution gives the semiconductor industry new insights into scaling low-k materials for several additional technology nodes."

More information: A paper describing the technique, “Three-

dimensional imaging of pore structures inside low-κ dielectrics," was published last week in Applied Physics Letters (June 2, 2010.)

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