SEMATECH Technologists Detail Process Advances to Accelerate 3D Manufacturing Readiness

April 21 2010

With a focus on providing cost-effective and reliable solutions to speed manufacturing readiness of 3D technology options, experts from SEMATECH's 3D interconnect program based at the College of Nanoscale Science and Engineering's (CNSE) Albany NanoTech Complex outlined new developments in wafer bonding, copper removal, and wafer thinning at the 2010 Materials Research Society (MRS) Spring Meeting on April 5-9 in San Francisco, CA.

3D integration offers the promise of higher performance, higher density, higher functionality, smaller form factor, and potential cost reduction. In this emerging field, new and improved technologies and integration schemes will be necessary to realize 3D's potential as a manufacturable and affordable path to sustaining semiconductor productivity growth. At MRS, SEMATECH researchers described several practical 3D integration achievements - applicable across various 3D processes - in areas such as high-aspect ratio TSVs, wafer bonding, and thinning of interconnect test structures.

"Through collaborative research, our goal is to develop and characterize new approaches to implementing 3D," said Sitaram Arkalgud, director of SEMATECH's 3D Interconnect Program. "These practical approaches are critical to the integration, process development, metrology, and tool sets that will make 3D TSVs commercially viable."

"The SEMATECH-CNSE partnership continues to drive leading-edge technologies that will accelerate 3D processes for manufacturing," said Richard Brilla, CNSE Vice President for Strategy, Alliances and Consortia. "This innovative research will enable critical advances to benefit our corporate partners and the global nanoelectronics industry."

In partnership with the UAlbany NanoCollege, specific SEMATECH process advances aimed at improving 3D performance include:

• A practical approach to copper overburden removal by chemical mechanical polishing (CMP), using high removal rate slurry screening and achieving good planarization results, with low polish defects, at a rate suitable for emerging 3D TSV copper applications.

• The process development and associated metrology necessary in thinning bonded 300mm TSV and non-TSV bonded wafers, leaving a defect-free surface which meets the requirements for subsequent processing.

• An array of metrology techniques used in characterizing a manufacturable wafer bond process to deliver a void and dendrite-free bond for handle wafers.

SEMATECH's 3D program was established at CNSE's Albany NanoTech Complex to deliver robust 300 mm equipment and process technology solutions for high-volume through-silicon via (TSV) manufacturing. To accelerate progress, the program's engineers have been working jointly with chipmakers, equipment and materials suppliers, and assembly and packaging service companies from around the world on early development challenges, including cost modeling, technology option narrowing, and technology development and benchmarking.

Source: SEMATECH