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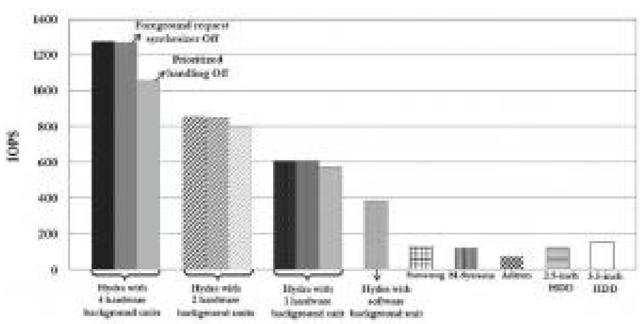
Hydra flash memory outperforms other top storage mediums

April 6 2010, By Lisa Zyga



This figure shows how Hydra's advantages, especially its multiple background units, compare favorably with other storage systems when emulating an online transaction processing system. Speed performance is measured in I/Os per second (IOPS). Image credit: Seong, et al. ©2010 IEEE.

(PhysOrg.com) -- Although today flash memory is primarily used as a removable storage medium, it's currently becoming more and more appealing for a wider variety of applications. Moving beyond memory cards and flash drives, flash memory solid-state disks (SSDs) are already beginning to replace the hard disk drives (HDDs) in mobile computing systems, such as tablets and notebook PCs. Taking another step in this direction, a team of researchers from Korea has recently integrated and tested several improvements into SSDs to create a new flash architecture called Hydra, whose performance has proven to be significantly better than several other storage mediums that the researchers examined.

In their study, researchers Yoon Jae Seong and coauthors from Seoul National University developed Hydra to take advantage of the parallelism of multiple flash memory chips. To do so, they used various design techniques that are well known in many areas of computing, but have not yet been extensively exploited in this type of SSD. The researchers' study will be published in an upcoming issue of *IEEE Transactions on Computers*.

"We believe that the Hydra architecture suggests an efficient way of exploiting parallelism inherent in multiple flash memory chips," Seong told *PhysOrg.com*. "The effects of design techniques such as interleaving, write buffering and prioritized handling are comprehensively analyzed using a prototype implementation."

As the researchers explain, Hydra helps to improve a few of the most troublesome shortcomings of NAND flash chips, which were designed primarily for bulk storage applications. NAND chips are organized into physical blocks, each of which contains many "pages." While the pages can be read and programmed individually, erasing must be done at the block level (electrons erase the data in a "flash," hence the name). Although this gives flash memory a faster access time than HDDs, it also means that, unlike HDDs, flash memory cannot directly overwrite existing data. In order to update data, flash must first erase the entire block and then reprogram each page in the block, which can be time-consuming. In addition, NAND flash is characterized by a slow bus, resulting in a slow transfer of data between the host and the memory.

Hydra attempts to minimize the effects of these problems with several strategies. First, Hydra arranges multiple NAND chips and buses into sets called "super-chips" to speed up the read and programming processes. As the researchers explain, memory operations are directed to a super-chip, which operates on a "super-block" (multiple blocks) and can span multiple "super-pages" (multiple pages). Thus, Hydra can operate on multiple chips simultaneously, which increases its speed. Similarly, four 40MB/s buses together can achieve a collective bandwidth of 160 MB/s, which meets or exceeds the maximum bandwidth of a typical host interface. The researchers also determined that multiple chips can hide the read latency that occurs during data transfer between pages, eliminating idle time.

Further, the researchers designed Hydra to have a prioritized structure of memory controllers, with a single high-priority unit that handles read requests from the host as quickly as possible, and multiple low-priority background units for other operations. If the high-priority unit needs to use a super-chip that is being used by a background unit, the high-priority unit can preempt the background unit as soon as possible. Having multiple background units also allows multiple super-chip operations to be performed in parallel, as long as they use different super-blocks. In addition, the researchers equipped Hydra with a volatile write buffering mechanism to ensure that these multiple flash memory chips are used as effectively as possible.

After implementing these new organizational features in a Hydra prototype, the researchers tested the SSD by comparing its performance to several other SSDs and HDDs. First, the researchers evaluated Hydra in a typical PC environment, where the memory was involved in tasks such as booting up Windows XP; loading applications such as Adobe Acrobat Reader, Microsoft Word, and the Mozilla internet browser; executing a variety of programs; performing a virus scan; and writing other files. The results showed that Hydra performed these tasks 80% faster than the best of five other disks that the researchers examined. In an evaluation of the same storage systems running an online transaction processing system, Hydra again outperformed the other systems in a similar way.

Further analysis showed which of Hydra's strategies were most effective for multiple concurrent tasks. Overall, the results showed that Hydra's additional low-priority background units proved to be the most effective enhancement.

Still, as Seong explained, SSDs face challenges, most notably cost and reliability.

"Especially, the reliability problem is getting worse as the geometry of NAND flash chips shrinks down further," he said. "Higher density NAND chips are more vulnerable to bit-flipping errors, and have lower retention and endurance."

Despite the challenges, the researchers hope that the insights from this study, along with the advantages of flash memory such as low power consumption and high shock resistance, will continue to make flash memory an appealing storage medium.

More information: Yoon Jae Seong, et al. "Hydra: A Block-Mapped Parallel Flash Memory Solid-State Disk Architecture." IEEE Transactions on Computers. To be published. Doi:10.1109/TC.2010.63

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