Graphene films clear major fabrication hurdle

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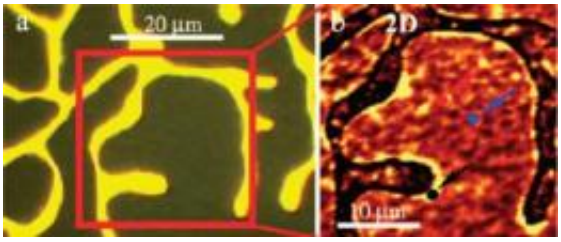


Panel (a): Optical image of a CVD graphene film on a 450 nanometer copper shows the finger morphology of the metal; (b) Raman 2D band map of the graphene film between the metal fingers, over the area marked by the red square on left. Credit: Image from Yuegang Zhang

Graphene, the two-dimensional crystalline form of carbon, is a potential superstar for the electronics industry. With freakishly mobile electrons that can blaze through the material at nearly the speed of light - 100 times faster than electrons can move through silicon - graphene could be used to make superfast transistors or computer memory chips. Graphene's unique "chicken wire" atomic structure exhibits incredible flexibility and mechanical strength, as well as unusual optical properties that could open a number of promising doors in both the electronics and the photonics industries. However, among the hurdles preventing graphene from joining the pantheon of star high-tech materials, perhaps none looms larger than just learning to make the stuff in high quality and usable quantities.

"Before we can fully utilize the superior electronic properties of graphene in devices, we must first develop a method of forming uniform single-layer graphene films on nonconducting substrates on a large scale," says Yuegang Zhang, a materials scientist with the Lawrence Berkeley National Laboratory (Berkeley Lab). Current fabrication methods based on mechanical cleavage or ultrahigh vacuum annealing, he says, are ill-suited for commercial-scale production. Graphene films made via solution-based deposition and chemical reduction have suffered from poor or uneven quality.

Zhang and colleagues at Berkeley Lab's Molecular Foundry, a U.S. Department of Energy (DOE) center for nanoscience, have taken a significant step at clearing this major hurdle. They have successfully used direct chemical vapor deposition (CVD) to synthesize single-layer films of graphene on a dielectric substrate. Zhang and his colleagues made their graphene films by catalytically decomposing hydrocarbon precursors over thin films of copper that had been pre-deposited on the dielectric substrate. The copper films subsequently dewetted (separated into puddles or droplets) and were evaporated. The final product was a single-layer graphene film on a bare dielectric.

"This is exciting news for electronic applications because chemical vapor deposition is a technique already widely used in the semiconductor industry," Zhang says. "Also, we can learn more about the growth of graphene on metal catalyst surfaces by observing the evolution of the films after the evaporation of the copper. This should lay an important foundation for further control of the process and enable us to tailor the properties of these films or produce desired morphologies, such as graphene nanoribbons."

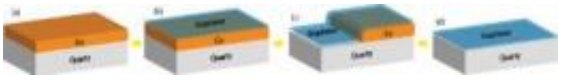
Zhang and his colleagues have reported their findings in the journal *Nano Letters* in a paper titled, "Direct Chemical Vapor Deposition of Graphene on Dielectric Surfaces." Other co-authors of this paper were

Ariel Ismach, Clara Druzgalski, Samuel Penwell, Maxwell Zheng, Ali Javey and Jeffrey Bokor, all with Berkeley Lab.

In their study, Zhang and his colleagues used electron-beam evaporation to deposit copper films ranging in thickness from 100 to 450 nanometers. Copper was chosen because as a low carbon solubility metal catalyst it was expected to allow better control over the number of graphene layers produced. Several different dielectric substrates were evaluated including single-crystal quartz, sapphire, fused silica and silicon oxide wafers. CVD of the graphene was carried out at 1,000 degrees Celsius in durations that ranged from 15 minutes up to seven hours.

"This was done to allow us to study the effect of film thickness, substrate type and CVD growth time on the graphene formation," Zhang says.

A combination of scanning Raman mapping and spectroscopy, plus scanning electron and atomic force microscopy confirmed the presence of continuous single-layer graphene films coating metal-free areas of dielectric substrate measuring tens of square micrometers.



To make a graphene thin film, Berkeley researchers (a) evaporated a thin layer of copper on a dielectric surface; (b) then used CVD to lay down a graphene film over the copper. (c) The copper dewets and evaporates leaving (d) a graphene film directly on a dielectric substrate. Credit: Image from Yuegang Zhang

"Further improvement on the control of the dewetting and evaporation process could lead to the direct deposition of patterned graphene for

large-scale electronic device fabrication, Zhang says. "This method could also be generalized and used to deposit other two-dimensional materials, such as boron-nitride."

Even the appearance of wrinkles in the graphene films that followed along the lines of the dewetting shape of the copper could prove to be beneficial in the long-run. Although previous studies have indicated that wrinkles in a graphene film have a negative impact on electronic properties by introducing strains that reduce electron mobility, Zhang believes the wrinkles can be turned to an advantage.

"If we can learn to control the formation of wrinkles in our films, we should be able to modulate the resulting strain and thereby tailor electronic properties," he says. "Further study of the wrinkle formation could also give us important new clues for the formation of graphene nanoribbons."

Provided by Lawrence Berkeley National Laboratory