15 Moore's Years: 3D chip stacking will take Moore's Law past 2020

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Some laws are made to be broken, and others are made to be followed. A team of IBM Researchers in collaboration with two Swiss partners are looking to keep one law in particular alive and well for another 15 years: Moore's Law. The law states that the number of transistors that can be placed inexpensively on an integrated circuit will double every 18 months. More than 50 years old, this law is still in effect, but to extend it as long as 2020 will require a change from mere transistor scaling to novel packaging architectures such as so-called 3D integration, the vertical integration of chips.

Making chips cool again

Last week, IBM, École Polytechnique Fédérale de Lausanne (EPFL) and the Swiss Federal Institute of Technology Zurich (ETH) signed a four-year collaborative project called CMOSAIC to understand how the latest chip cooling techniques can support a 3D chip architecture. Unlike current processors, the CMOSAIC project considers a 3D stack-architecture of multiple cores with a interconnect density from 100 to 10,000 connections per millimeter square. Researchers believe that these tiny connections and the use of hair-thin, liquid cooling microchannels measuring only 50 microns in diameter between the active chips are the missing links to achieving high-performance computing with future 3D chip stacks.

"In the United States, data centers already consume two percent of the

electricity available with consumption doubling every five years. In theory, at this rate, a supercomputer in the year 2050 will require the entire production of the United States' energy grid," said Prof. John R. Thome, professor of heat and mass transfer at EPFL and CMOSAIC project coordinator. 3D chip stacks with interlayer cooling not only yield higher-performance, but more importantly, allow systems with a much higher efficiency, thereby avoiding the situation where supercomputers consume too much energy to be affordable.

3D challenges

The CMOSAIC team faces a number of formidable challenges, but recent progress across all fronts is giving the research team confidence to move forward. For example, progress in the fabrication of through-silicon vias has opened new avenues for high-density-area array interconnects between stacked processor and memory chips. Such 3D-integrated circuits are extremely attractive to overcome the bandwidth bottleneck between core and cache memory, offering an opportunity to extend the CMOS performance and efficiency trends for another decade.

By integrating a very large system on a chip (SoC) in multiple tiers, the average distance between system components is reduced, which will improve both efficiency and performance. However, the challenge to remove the heat generated as chip volumes become smaller and smaller is now the key issue. The overall concept is counterintuitive: the higher power densities we can allow, the higher the efficiency of a future system.

To solve the cooling challenge, the team is leveraging the experience of IBM and ETH in the development of Aquasar, a first-of-a-kind, water-cooled supercomputer.

Similar to Aquasar, the team plans to design microchannels with single-phase liquid and two-phase cooling systems using nano-surfaces that pipe coolants—including water and environmentally-friendly refrigerants—within a few millimeters of the chip to absorb the heat, like a sponge, and draw it away. Once the liquid leaves the circuit in the form of steam, a condenser returns it to a liquid state, where it is then pumped back into the processor, thus completing the cycle.

"As we will demonstrate with ETH in the Aquasar project, employing microchannels carrying liquid coolants offers a significant advantage in addressing heat-removal challenges, and this should lead to practical 3D systems," said Bruno Michel, manager advanced thermal packaging, IBM Research - Zurich. "Water as a coolant has the ability to capture heat about 4,000 times more efficiently than air, and its heat-transporting properties are also far superior." Chip-level cooling with a water temperature of approximately 60°C is sufficient to keep the chip at operating temperatures well below the maximally allowed 85°C. The high input temperature of the coolant results in an even higher-grade heat as output, which in this case will be about 65°C.

More information: Moore's Law - en.wikipedia.org/wiki/Moores_law

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