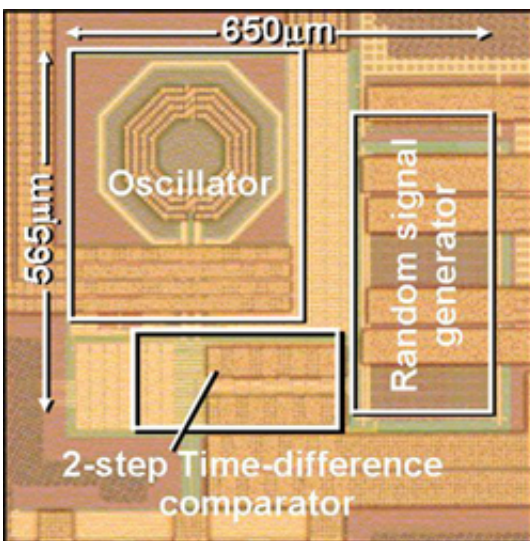


# NEC Develops 'Low-Power, Low-Noise All-Digital Phase Lock Loop' for Portable Wireless Terminals

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The structure of newly developed ADPLL LSI.

NEC Corporation today announced a development of the "Low-Power Low-Noise All-Digital Phase Lock Loop (ADPLL)" LSI. The newly developed LSI is suitable for midget wireless equipment yielding a long operation lifetime for small-sized batteries. It also features low-phase noise, which is vital to many modern wireless systems, including Bluetooth, ZigBee, WiFi, and WiMAX.

Features of the new PLL circuit:

1. Suitable for intermittently operated wireless equipment owing to the low-operation current and short lock-up time (recovery time from sleep mode) of 8.1 milliamperes (mA) and 20 microseconds, respectively. Operation lifetime for small-sized batteries can be as long as several years even for over-Mbps wireless transmission applications.
2. Low-phase noise of -105 dBc/Hz in the frequency range of 2.1 GHz to 2.8 GHz being compatible with a wide variety of modern wireless systems.
3. Small macro area of  $0.37 \text{ mm}^2$  including an on-chip Loop-Filter.

In recent years, there are increasing demands for short distance radio communication, such as remote controllers, alarm systems and automatic meter reading. [Power consumption](#) is one of the primary concerns of these systems in terms of long battery life. To keep the wireless module as small and lightweight as possible, severe restrictions are being imposed on battery size. As the battery size is reduced, the battery capacity also decreases, thus reducing the total available energy. Long battery life over several years is a desirable feature for these applications as it allows users to become free from battery replacement tasks.

For battery driven devices, intermittent operation is effective for extending battery life. However, analog-based PLL is not suitable for intermittent operations due to its long start-up time. In this regard, all-digital PLLs that allow quick operations are more suitable, together with their additional advantage of eliminating large on-chip passive filters. However, there are challenges to simultaneously achieving both the low power consumption and the low phase noise that are required in modern high-speed wireless systems.

The key building block of the newly designed ADPLL, the TDC (Time-to-Digital Converter), has a new architecture that can achieve high

accuracy in time-domain signal processing with reduced power consumption: the novel architecture is based on a fine/coarse two-step phase comparison scheme that can greatly reduce the number of circuit elements to be powered in each timing-comparison step. Using such a scheme, only a fraction of the PLL circuit is powered, minimum time is required and the other circuits are automatically shut down. Meanwhile, in order to achieve a low phase noise for ADPLL, another novel design is employed that intentionally adds a random signal to the oscillator. This approach drastically suppresses undesired noise originating from digitally periodic control. Based on these two developments, the digital PLL technique is now made applicable to a high-speed wireless system that simultaneously requires low-noise and extremely low-power performance.

The new all-digital PLL has the world's lowest power consumption, making it ideal for use in battery powered portable wireless equipment. These results can also be applied to RF chips in support of any wireless standard.

NEC and NECEL presented the results of this research on February 10 at the IEEE International Solid State Circuits Conference (ISSCC 2010), held between February 7 - 11 in San Francisco, California, U.S.A.

Source: NEC

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