Applied Materials Introduces Critical Via Liner Technology for 3D Chip Packaging

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Using a unique CVD process, the new Applied Producer InVia system delivers an innovative method for depositing the critical oxide liner film layer in high aspect ratio TSV structures.

Applied Materials, Inc. today added to its extensive line of 3D chip packaging solutions with the launch of its Applied Producer InVia dielectric deposition system. Using a unique CVD process, the InVia system delivers an innovative method for depositing the critical oxide liner film layer in high aspect ratio (HAR) through-silicon via (TSV) structures. Providing conformal coverage over the full depth of these challenging features, the InVia process enables robust electrical isolation of the TSV - which is vital for reliable device performance.

TSVs play a key role in emerging 3D packaging schemes, electrically

connecting chips that are vertically stacked to boost speed and lower power consumption. Two primary techniques, called via-first and via-middle, in which the TSVs are fabricated along with the device's transistor and interconnect layers, offer superior design flexibility and device functionality, but have presented a significant challenge for insulating liner processes. The InVia system's proprietary process technology meets the challenges of both techniques, depositing uniform, thick oxide films in greater than 10:1 HAR vias while meeting thermal budget requirements.

Implemented on Applied's Producer GT platform, the InVia system offers compelling advantages over competing technologies. The system has much higher throughput than batch furnaces, with the capability to process up to eight times more wafers per hour at less than half the cost, especially when depositing very thick liners for high performance applications. Competing PECVD systems are unable to deposit oxide films evenly in deep, narrow vias, making this approach unsuitable for HAR applications.

"With the launch of the InVia system, we now provide customers with a comprehensive solution for fabricating high aspect ratio TSVs," said Bill McClintock, vice president and general manager of Applied's DSM and CMP business unit. "From etch and via liners, to metal fill and planarization, we can offer chip manufacturers a cost-effective, rapid path to implement their most challenging 3D packaging schemes and quickly bring their exciting new products to market."

More information: For more information on Applied's range of systems for 3D chip packaging applications, visit www.appliedmaterials.com/3d_integration .

Source: Applied Materials

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