Researchers Develop World's First Digitally-Processed Gigabit-Class High-Speed Transceiver Chip

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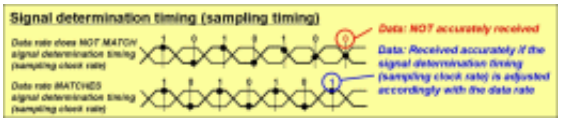

Automatic self-adjustment of signal-determination timing.

Fujitsu Laboratories and the University of Toronto announced their joint development of a new processing method for transceiver chips used in gigabit-class high-speed data transmission over wirelines.

The new technology employs digital circuitry to replace previously-required structures that used analog circuits. While analog processing require circuits that are adapted to the specifications of a signal being transmitted, such as transmission distance and amplitude, this new digital approach can perform these optimizations automatically, so that a single circuit could be used to accommodate a wide range of various wireline communications. Compared to conventional processing methods, this new digital-processing method makes it possible to shorten development periods by approximately half. It is anticipated that this new technology in the future could be applied to a variety of wireline communication applications, including 10 Gbps high-speed Ethernet in datacenters.

Details of this technology were presented at the IEEE International Solid-State Circuits Conference 2010 (ISSCC 2010) being held in San Francisco from February 7-11.

File size data volumes for large photographic, audio, and video files are becoming increasingly larger, thus requiring a significant amount of bandwidth to transmit, leading to demand for ever-faster wireline data communications. Conventional transceiver chips rely on analog circuitry which needs to be optimized to accommodate specifications of the signal being transmitted — such as transmission distance and amplitude — and therefore require multiple transceiver chips to be designed in order to accommodate for various applications.

With a growing diversity of devices featuring high-speed data transmission, the need to optimize an existing technology for every new type of device or model has become a bottleneck in the development process. Efforts to develop transceiver chips within short development periods that can accommodate the wide range of different devices have been proven challenging.

Fujitsu Laboratories and the University of Toronto have developed a digital circuit-based transceiver chip. Featuring digital circuitry, the new transceiver chip can automatically optimize itself for a variety of high-speed communications circuits, thus significantly reducing development periods by approximately half compared with conventional methods.

Automatic self-adjustment of signal-determination timing is a key feature of the new technology.

This technology detects variations in the delay on the time axis of the input signal, caused during data transmission, and based on that can automatically adjust the timing it uses for judging whether an incoming signal is a 0 or 1 (Figure 1, see above). Since variations in data

transmissions increase along with faster transmission speeds, this new technology is essential for accurate data exchange. This is the world's first technology to achieve Gbps-class speeds without the use of analog circuitry elements, while offering fully-digital timing adjustments for signal-determination.

Waveforms traveling over a cable degrade, but sophisticated digital-signal processing can compensate for the degraded waveforms (Figure 2).

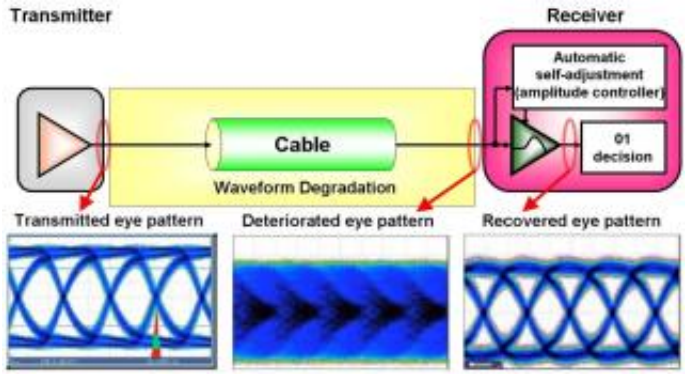

Figure 2. Automatic compensation of signal-quality degradation over transmission circuits.

As a world's first, by using digital circuitry-based high-speed transceiver technology, Fujitsu Laboratories and the University of Toronto's new technology makes it possible to reduce the design and development period for a gigabit-class transceiver chip by approximately one-half (1/2) compared with conventional methods. This suggests that transceiver chips for a wide range of communications devices could be offered in a timely manner.

Researchers plan to continue with development of this technology to

optimize the digital signal processing, to further reduce the transceiver's power consumption.

Source: Fujitsu