Toshiba Develops SRAM Circuit Technique that Secures Low Voltage Operation of System LSI

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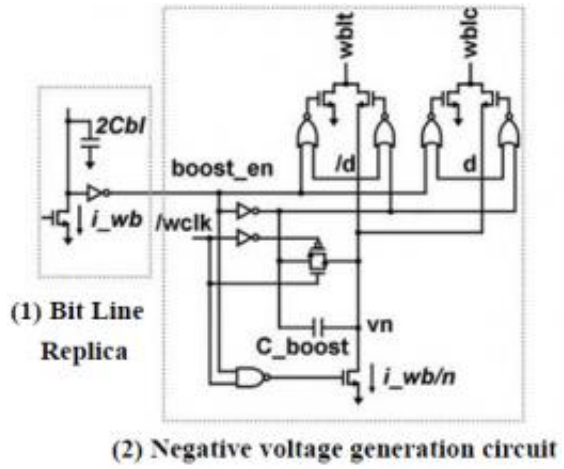
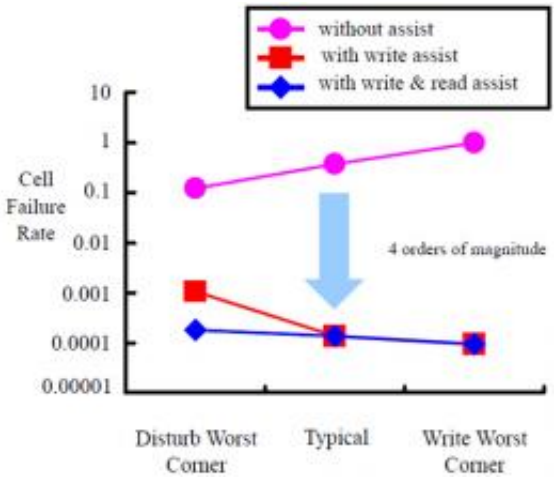


Toshiba eliminated the need for circuit adjustment by developing a scheme to determine the operation timing of the negative voltage generation circuit (2) based on the length of the Bit Line Replica (1). This supports simplified, software-based generation of SRAM design data according to memory capacity and the cell array configuration.

Toshiba Corporation today announced that it has developed a breakthrough technology that achieves low voltage operation of System LSI, opening the way to reduced power consumption in digital products. The technology secures successful operation of static random access memories (SRAM) at low voltage with an improved circuit design that optimizes voltage control of the bit line and word line.

The new technology overcomes the high failure rate that has been the main challenge in achieving practical, low voltage SRAM, and reduces memory cell failure rate by four orders of magnitude at 0.7V. Moreover, the circuit design can be applied to the memory compiler, software that automatically configures SRAM, contributing to shorter design lead times and bringing an effective solution to the LSI development process.

Toshiba will unveil the new technology on the fourth day of the 2010 International Solid State Circuit Conference (ISSCC), one of the semiconductor industry's leading international conferences, which is being held in San Francisco, California, U.S.A., from February 7 to February 11.



Impact on cell failure rates

System LSI is the core components of digital products, and their operation voltage has a major impact on power consumption(1). However, voltage scaling of cutting-edge system LSI has been a big challenge, because embedded SRAM lose stability in the memory function at low voltage. The memory cell transistors of SRAM are

smaller than those of other logic circuits, which makes SRAM operation susceptible to transistor variability at low voltage (2).

Toshiba has overcome this problem with a new method that employs read-assist and write-assist techniques and secures the function of a low voltage SRAM.

Read-assist and write-assist techniques are recognized as a means to stabilize SRAM functionality by optimizing bit-line and word-line level during read and write operation. However, the conventional write-assist technique requires adjustment in circuit parameters of the SRAM's negative voltage generator to match the SRAM capacity. This has been an obstacle to design efficiency and has hindered practical application.

Toshiba's novel solution employs a newly developed negative voltage generator with bit-line-capacitance replica, which adaptively optimizes the negative level to the SRAM capacity. This approach eliminates the burden of adjusting circuit parameters in accordance with the SRAM configuration by automating the SRAM design process.

Toshiba has confirmed this highly significant advance by measurement: a test chip fabricated with 32-nanometer high-k/metal gate process technology cut voltage for stable operation from the 1V typical for conventional SRAM to 0.7V. Equally as significant, the failure rate decreased by four orders of magnitude, i.e. a 10,000 times improvement.

Other approaches proposed for securing SRAM stability employ a memory cell that increases the transistor count from the typical number of six. However, Toshiba's approach is more efficient, as it requires no increase in transistors, avoiding the penalty of an increase in the SRAM cell area.

Cutting-edge system LSI is designed to use a supply voltage around 1V.

However, further reductions in set power consumption require much lower voltages. Toshiba will continue to promote early development of practical, low voltage circuit techniques and advanced CMOS technology toward the goal of achieving high performance system LSI that consumes less power.

More information: (1) An LSI's active power consumption is proportional to the square of the supply voltage. For instance, if supply voltage were reduced from 1.0V to 0.7V (by 30%), power consumption is decreased by approximately 50%.

(2) Since the threshold voltage of smaller transistors experiences greater variability, an SRAM cell integrating small transistors is subject to large variations in operating characteristics, particularly in low voltage operation.

Source: Toshiba Corporation

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