Scatterometry -- measuring ever-smaller chip production

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(PhysOrg.com) -- As computer chips rapidly continue to evolve, new technologies must be developed to closely monitor the fabrication process and guard against faults at a sub-microscopic level.

More than 40 years ago Intel co-founder Gordon Moore predicted the capacity of computer chips would double every two years for a 10-year period. He was wrong about the time, but right about the rest. Despite frequent reports and predictions of its demise, Moore's law is still going strong today.

The development of a host of new technologies enabling ever-increasing miniaturisation has resulted in a new generation of smaller, smarter chips coming to market approximately every two years.

The current generation of chips measures just 45 nanometres (nm). In 1990, state-of-the-art chips measured 800nm, and in 2000 this was down to 180nm. However, the next generation of chips which manufacturers are working on now will measure just 32nm with 22nm expected two years later and 16nm two years after that.

Alongside the techniques which allow an increasing number of transistors to be placed on an integrated circuit, a new set of techniques also has to be developed to allow the measuring of fault tolerance on a tiny scale.

And the jump from 45nm to 32nm is such that entirely new techniques are required, because the existing way of checking for faults on chips may not be accurate enough at this new level.

To overcome this problem, an EU-funded project, SOCOT, was set up bringing together a vendor of metrology - measuring - tools, a software developer with experience in metrology, a chip manufacturer and an R&D centre.

Project coordinator Daniel Kandel says measuring for faults has always been a key part of the chip-making process but the EU project was necessary “because there was a significant risk that, at 32nm, no existing technology could measure the alignment between layers with sufficient precision and accuracy.” He points out a 32nm wide line is only the width of 59 silicon atoms - silicon being the main material for making the wafers the chips are embedded in.

One of the most important measurements is the alignment between the numerous layers which make up semiconductors. The maximum error the manufacturer is prepared to accept is known as the overlay control budget.

With the 45nm generation of chips, the budget allowed for an error is 10nm. This came down from 12nm with the previous generation with similar gradual reduction from earlier generations. But the evolution from 45nm to 32nm technology has seen the need for a much sharper jump in alignment requirements, from 10nm to 3nm.

“The measurement accuracy is typically one-tenth of the error that can be tolerated, so in this case the metrology has to be accurate to 0.3nm or 3 angstroms,” says Kandel.

Whole new approach... scatterometry

This sudden reduction between the current and next generation has meant the technology used for measuring this and previous generations of chips may no longer be effective. The problem is that current technology involves looking at images of patterns on adjoining layers with a very powerful microscope. The images show what, if any, misalignment there is between the two layers.

But with the alignment requirements now being equivalent to the width of a small number of atoms, even the most powerful microscope is not able to achieve this level of accuracy and precision and so imaging overlay technology may no longer be viable.

The researchers realised a whole new approach was needed and decided to experiment with scatterometry, a new technique which is already in use for other types of measurement in chip-manufacturing facilities.

“With scatterometry you do not need an image, you simply scatter light,” explains Kandel. “Using the measuring tool we have developed, you illuminate the wafer with light of a variety of wavelengths and then measure the scattered light. We have developed sophisticated software programs or algorithms which allow us to calculate the level of

misalignment from the light signatures," he says.

Scatterometry has other advantages over techniques that employ microscopes, because images are sensitive to the optical quality of the lenses which can produce optical aberrations. Imaging technology is also sensitive to the focus of a microscope which can easily be set too high or low. Scatterometry is insensitive to errors in focus or the optical quality of the tool being used.

The project's researchers initially set up simulations to confirm their projections could be met, and then they built a prototype tool to achieve optimal architecture and performance. This was demonstrated in an R&D environment and a misalignment measure of 3 angstroms accuracy was achieved.

"We showed you could perform this type of measurement, and control the process using the results obtained and that is where the project ended," says Kandel.

However, the work done in SOCOT lives on and the next generation of measuring tools will be based on the technologies researched in the project. "Chip-makers will be able to buy a commercial product to use in their facilities when they switch to next-generation manufacturing," he says.

Initially, he expects the technology to be used only in the most critical layers where tolerances are very tight. However, they will last through the next few generations of chips and more layers will be measured in this way at the 22nm and 16nm levels.

More information: SOCOT project -- www.socot-overlay.org/

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