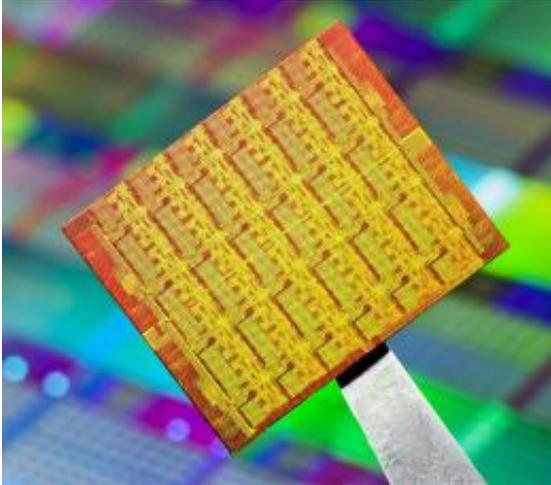


Intel's single-chip cloud computer

February 11 2010, by Lin Edwards



Single Chip Cloud Computer has 48 Intel cores and runs at as low as 25 watts.

(PhysOrg.com) -- Intel Labs has recently shown off a 48-core prototype chip it calls a "single-chip cloud computer" or SCC.

Chief technology officer with [Intel](#), Justin Rattner, said [the chip](#) comprises 1.3-billion transistors arranged in a network of 24 tiles, each of which has two Pentium-class IA-32 cores, two L2 caches, plus a router to enable communications between cores. The system uses new software applications to control the power consumed by the cores, and to rapidly transfer data between the cores. This means data can go directly between cores without needing to go via the main memory, and this cuts the data transfer speed by 15 times. The software prevents the data being corrupted by instructing the cache sending the data to delete its copy

after it is sent, and the receiving cache to delete old copies of the data before receiving the new.

The software controlling power consumption allows application developers, rather than the operating system, to decide how power consumed by the cores is controlled. The tiles can all be independently controlled, which means the [power consumption](#) on some cores can be reduced to as low as 25 watts, while others can be up to 125 watts. While some developers are not yet sure what they will do with the feature, many are interested in learning more.

Intel's director of advanced microprocessor research, Nitin Borkar, said tasks could be programmed to run at greater [power efficiency](#) rather than higher power if appropriate, or individual cores could be throttled back after they have finished their computations. This would give the system the "compute on demand" feature of traditional data centers.

Intel Labs are forming partnerships with industry and university researchers and producing 100 of the chips to enable research to refine the [chip](#) architecture and maximize its usefulness.

The chip was unveiled at the [IEEE International Solid-State Circuits Conference](#) in San Francisco on 8 February.

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