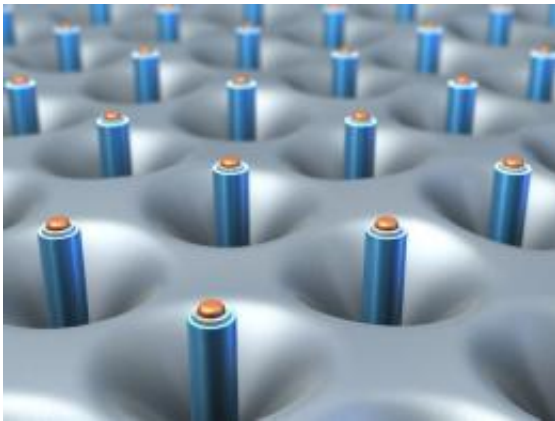


High, not flat: nanowires for a new chip architecture

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Scheme of a silicon wafer with novel vertical transistors made out of silicon nanowires

Nowadays, a myriad of silicon transistors are responsible to pass on the information on a microchip. The transistors are arranged in a planar array, i.e. lying flat next to each other, and have shrunk down already to a size of only about 50 nanometers. Further miniaturization of transistors with a planar structure will soon come to an end due to fundamental physical limits. Still, even smaller transistors are desirable in order to continuously improve their functions while reducing the cost of the electronics.

Currently, researchers are working hard to find new approaches to overcome the physical limits on downscaling and integration of

microchips. One such concept is to fabricate a completely new transistor architecture in three-dimensions. In this concept, instead of arranging them flat on the substrate the [silicon transistors](#) are turned by 90 degrees so that they stick out of the chip substrate like tiny columns. In this way, numerous vertical transistors could be built on the area normally occupied by only one planar transistor. This would finally be the step from micro to nanoelectronics.

The fabrication of vertical silicon nanowire arrays has already been reported. Yet there needs to be a more thorough research into the [electrical properties](#) of silicon nanowires in order to be able to build reliable transistors for a new generation of microchips. Unlike conventional transistors, the current flow in these column-like transistors will be vertical, and they will be smaller and more energy-saving than today. Last but not least, there are high hopes to fabricate extremely efficient [solar cells](#) using silicon nanowires.

The Max Planck researchers in Halle produce monocrystalline silicon nanowires which are particularly suitable as components for microchips. At the FZD's [ion beam](#) center, foreign atoms known as 'dopants' are implanted into the nanowires. The dopants occupy lattice sites of the host semiconductor increasing the electrical conductivity and the current flow through the semiconductor. Selective implantation of different dopants can change the polarity of the charge carriers in a transistor leading to the switching of the current flow. The planar silicon technology is well developed; however, this is not true for silicon nanostructures. "First, we analyzed wires with a diameter of 100 [nanometers](#) and 300 nanometers in length. But what we aim at are wires with a diameter of a few atoms only, as well as wires where individual atoms are strung together. We intend to closely characterize their behavior in materials and want to find out how their electrical properties can be tailored for application in nanoelectronics, e.g. for new field-effect transistors," say FZD physicists Dr. Reinhard Koenig and Dr. Xin

Ou.

The nanowires were investigated in Rossendorf using a technique (Scanning Spreading Resistance Microscopy, SSRM) that usually measures the position- dependent electrical resistivity in a specially-prepared two-dimensional cross-section of the nanowire. The resistivity is related to the atomic concentration of the dopants. In the current work, the researchers have found that the dopants in a silicon nanowire, namely boron and phosphorus, do not stay where they are expected, but drift to the surface of the nanowire where they become partially inactive and can no longer contribute to the [electrical conductivity](#). Up until now scientists were lacking an appropriate technique to visualize and quantify the consequences of an unequal distribution of dopants at the nanoscale. Chip designers have to pay attention to the newly found results if [nanowires](#) are to be applied for vertical transistors in the future.

More information: “Carrier Profiling of Individual Si Nanowires by Scanning Spreading Resistance Microscopy“, *Nano Letters* 2010,10,171-175,
[DOI:10.1021/nl903228s](https://doi.org/10.1021/nl903228s)

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