New simulation tool could shorten manufacturing design process

January 28 2010

Novel research on improving the simulation performance of hardware models created in a language called SystemC, often used to shorten manufacturing design cycles to improve the time it takes to bring a product to the marketplace, has garnered a best paper award at the 15th Asia and South Pacific Design Automation Conference (ASP-DAC) for a team led by Sandeep Shukla, Virginia Tech associate professor of electrical and computer engineering (ECE), and three of his students.

Shukla, a 2004 recipient of a Presidential Early Career Award for Scientists and Engineers (PECASE) and a 2008 recipient of the Freidrich Wilhelm Bessel Award from the Humboldt Foundation of Germany, wrote the paper with his current Ph.D. students, Mahesh Nanjundappa and Bijoy A. Jose, also of Virginia Tech, and a past Ph.D. advisee Hiren D. Patel who is now an ECE assistant professor at the University of Waterloo in Canada.

Shukla and his collaborators said that they were able to demonstrate how to speed up the simulation performance of certain SystemC based hardware models "by exploiting the high degree of parallelism afforded by today's general purpose graphic processor units (GPGPU)." These units have multiple core processors capable of very high computation and data throughput. When parallelism is applied, it means that the processor units can run various parts of the simulations simultaneously, and not just as a single sequence of computations. Their experiments were carried out on an NVIDIA Tesla 870 with 256 processing cores. This equipment was donated to Shukla's lab by NVIDIA during fall

2008.

Shukla said their preliminary experiments showed they were able to speed up SystemC based simulation by factors of 30 to 100 times that of previous performances.

They named their simulation infrastructure SCGPSim. The Air Force Office of Scientific Research and the National Science Foundation helped support this research.

In the past, Shukla said, "significant effort was aimed at improving the performance of SystemC simulations, but little had been directed at making them operate in parallel. And none of the attempts were ever targeted at a massively parallel platform such as a general purpose graphic processor unit."

Another aspect of their work was the use of a specific programming model called Compute Unified Device Architecture (CUDA). It is an extension to the C software language that "exploits the processing power of graphic processor units to solve complex compute-intensive problems efficiently," Shukla explained. "High performance is achieved by launching a number of threads and making each thread execute a part of the application in parallel."

The CUDA execution model differs from the more commonly known central processing unit (CPU) based execution in terms of how the threads are scheduled. With CUDA, it is possible to have all of the threads execute simultaneously on separate processor cores and intermittently converge on the same path, thus increasing the efficiency.

The work at Virginia Tech was conducted in the Formal Engineering Research with Models, Abstractions and Transformations (FERMAT) Laboratory, founded by Shukla in 2002. Its focus is in designing,

analyzing and predicting performance of electronic systems, particularly systems embedded in automated systems.

"Speeding up simulation of complex hardware models is extremely important for semiconductor electronics industry to producer newer and newer products in shorter times, thus improving the quality of computing and consumer electronics products faster. If such models can be simulated 10 times faster, then if validating a model took 10 days in the past, now it would take one day. This is why faster simulation performance probably attracted the attention of the ASP-DAC '10 awards committee." Shukla said.

More information: http://www.asp-dac.itri.org.tw/aspdac2010/awards/index.html

Provided by Virginia Tech