Toshiba Develops High Performance CMOS Device Technology for 20nm Generation LSI

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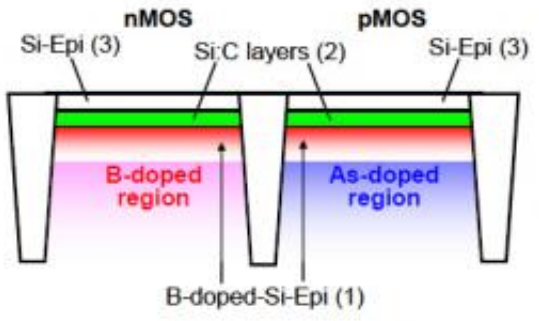

(PhysOrg.com) -- Toshiba Corporation today announced that it has developed a breakthrough technology for steep channel impurity distribution that delivers a solution to a key problem for 20nm generation CMOS technology. The technology opens the door to a future generation of LSI fabricated with bulk CMOS technology, the mainstream technology in today's LSI, by achieving the world's first practical fabrication process applicable to 20nm generation CMOS devices.

Toshiba unveiled the new technology at the 2009 International Electron Devices Meeting (IEDM) held in Baltimore, Maryland, U.S.A. from December 7 to December 9, one of the semiconductor industry's leading international conferences.

The new technology forms three layers on the surface of the channel: epitaxial silicon (Si), carbon-doped silicon (Si:C), and boron-doped Si:C. The top epitaxial Si layer functions as a low resistance path for the electrons and the holes; the intermediate Si:C acts as a defensive layer to prevent impurity diffusion; and the bottom boron-doped Si:C layer suppresses the fixed charge caused by the Si:C layer formation. Toshiba has confirmed that application of this novel structure achieves a boost in performance surpassing that of the conventional channel structure by 15 to 18%. This structure can be applied to both the nMOS and pMOS transistors to configure CMOS devices, with a simple process that adds a few layer-forming steps.

Previous R&D efforts have largely focused on nMOS transistors, in which channel impurities diffuse easily, or on examining the introduction of new solutions, such as SOI wafers and a 3D gate structure. Toshiba's new technology realizes a high-performance 20nm generation process without employing such new solutions, simply by optimizing impurity materials, device structures and processes.

Background and Targets

Today's bulk CMOS technology is seen as facing physical limits at around the 20nm generation. Problems such as degradation in electron mobility in the channel area and variation in threshold voltage will become obvious at that scale. These problems can be overcome by realizing a steep impurity distribution in the channel area, a structure that requires a low impurity density surface layer and a high impurity density substrate layer. This structure contributes better gate electrode control over the low-resistance area on the surface by obtaining fine switching of the current.

R&D in steep channel impurity profiles has largely been limited to the partial optimization of nMOS transistors, in which channel impurities

easily diffuse, and effective technologies that can secure the overall CMOS performance in the 20nm generation has been a big challenge. As a result, the industry's attention has been directed to new materials or device structures, such as SOI wafers and a 3D gate structure. However, these solutions may result in new process steps that require extra facility investment or that lower productivity. Toshiba's newly developed technology , which is applicable to both the nMOS and pMOS transistors of CMOS devices, opens the way to taking bulk CMOS technology forward to the 20nm generation.

Brief overview

1. Conditions of development

The following technologies are necessary to create a steep channel profile:
(a) A silicon layer formed on the surface of the channel after introducing impurities into the channel area.
(b) A structure that prevents impurity diffusion to the surface due to thermal budget generated during the fabrication process.
(c) Optimization of materials and structures so that the channel functions effectively.

To develop a CMOS device, these technologies are necessary for both the nMOS and pMOS transistors. Although optimization of nMOS has been already achieved, integration of CMOS devices with optimized pMOS has not followed.

2. New achievement

Toshiba has extended the nMOS results to develop both nMOS and pMOS devices as shown below. Performance has been confirmed to be

15 to 18% higher than that achieved with the conventional channel structure. Key points are in the followings;
(1) A boron-doped Si:C layer is formed in advance of the Si:C interlayer formation. For the pMOS device, arsenic is used to dope the channel.
(2) An Si:C interlayer is formed for both the nMOS and pMOS devices.
(3) Finally, a silicon layer is formed on the channel surface by epitaxial growth, for both the nMOS and pMOS devices.

Toshiba has optimized both the materials and the structures to realize an efficient fabrication process. Arsenic has been confirmed as a potential candidate for the pMOS channel impurity. In the pMOS device, unwanted fixed charge accumulation in the gate insulator, due to the carbon in the Si:C layer, is resolved by adding a boron-doped silicon layer under the Si:C layer. This result is achieved by making efficient use of the interaction between carbon and boron.

Source: Toshiba Corporation