Glasgow scientists predict the unpredictable to guide future nano-chip design

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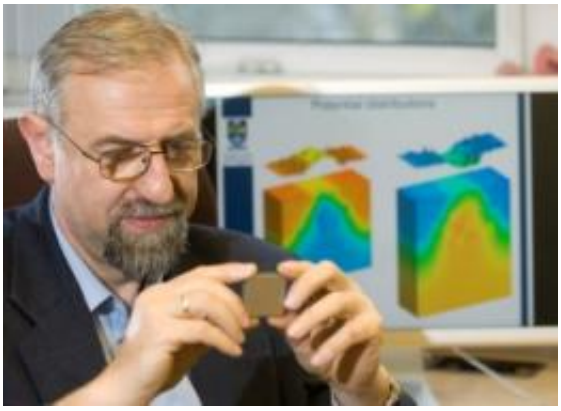

Scientists at the University of Glasgow, in collaboration with colleagues from Edinburgh, Manchester, Southampton and York universities, have developed technology which will help microchip designers create future integrated circuits.

As part of a £5.3m Engineering and Physical Sciences Research Council (EPSRC) eScience pilot project called NanoCMOS they have developed simulation tools which take advantage of grid computing to predict how billions of nano-transistors, each with their own unique and unpredictable atomic-scale variations, will perform within a circuit.

The simulations will help tackle the problem of 'statistical variability'

within transistors which is a major obstacle in the continued scaling of Complementary Metal-oxide Semiconductor (CMOS) microchips in future nano-scale technology generations.

Professor Asen Asenov, who is the principal investigator of NanoCMOS and leads the device modelling team at Glasgow which developed the simulation tools, said: “Nano-scale transistors are at the heart of our computers, mobile phones, cars, TV sets and games consoles chips. They play a crucial role in the UK vision for the digital economy of the future.

“Since their invention in 1947, they have been getting smaller and smaller so that today we can place billions of transistors onto one small sliver of silicon.”

Transistors today have gate lengths of 40 nanometres; by comparison a human hair is around 100,000 nanometres wide. However, the smaller they become, the more atomic-scale imperfections and variations within each transistor become a problem.

Statistical variations between transistors mainly occur due to the random number

and position of discrete dopants - chemical spices introduced in the silicon of which the microchips are made to form the structure of the individual transistors.

This statistical variability means that circuits built from billions of transistors with individually-unique properties may not perform as well as expected, despite being manufactured in an identical way.

Prof Asenov said: “If we are to continue to shrink the size of transistors in order to develop ever more powerful circuits, we need fundamentally

new approaches to circuit and system design that can take account of the statistical variability.

“Up until now, Moore’s Law, the prediction made in 1965 by Intel co-founder Gordon Moore that transistor dimensions will scale continuously and the number of transistors that could be placed on a microchip would double every two years, has been the driving force of the chip manufacturing and design industry, but the days of ‘happy scaling’ are over.”

However, Prof Asen Asenov and his team have applied grid computing technology to tackle the problem in the framework of NanoCMOS, funded by the EPSRC, in collaboration with leading design houses, chip manufacturers and software vendors.

Using grid computing technology, simulations of huge numbers of microscopically different nano-transistos have been carried out on thousands of microprocessors on networked computer clusters consuming more than 20 years’ of CPU time in a week. As a result the team are able to accurately predict for the first time, using three-dimensional numerical simulations, how billions of microscopically different transistors will perform in future computer chips.

The 3D simulations provide the scientists with information on the statistical distribution of the transistors characteristics helping to predict how many of the transistors in a silicon chip will work. This information allows the chip designers to design reliable chips out of variable and unreliable transistors.

Results of the simulation of unprecedented numbers of transistors will be presented at the International Electron Devices Meeting in Baltimore in December. Complementary results were also published in the October edition of leading electronics device journal ‘IEEE Transaction on

Electron Devices'.

Prof Asenov added: "The NanoCMOS project has helped not only to understand, for the first time, intimate details of statistical variability, but also to develop enhanced algorithms that will allow accurate prediction of statistical variability with greatly reduced computational efforts.

"This will be a great benefit, not only to the major semiconductor manufacturers around the world, but also to the vibrant UK chip design industry that is facing the increasing challenges of the modern nano-CMOS technology and design."

The NanoCMS grid computing technology was developed by the National e-Science Centre at the Universities of Glasgow and Edinburgh and the e-science North West Centre at Manchester University.

Provided by University of Glasgow