IBM Announces Highest Performance Embedded Processor for System-on-Chip Designs

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IBM today announced the industry's highest performance, highest throughput processor for system-on-chip (SoC) product families in the communication, storage, consumer, and aerospace and defense markets.

LSI Corporation has collaborated with IBM on the development of the processor core, called the PowerPC 476FP. LSI intends to utilize the 476FP PowerPC core in its next-generation multicore platform architecture for networking applications.

The PowerPC 476FP operates at clock speeds in excess of 1.6 GHz, and 2.5 Dhrystone MIPS (million instructions per second) per MHz, delivering over two times the performance of IBM's most advanced embedded core currently available for the original equipment manufacturing (OEM) market. This level of performance also positions the 476FP as the highest performing embedded processor for System-on-Chip designs yet announced and available in the industry.

The processor extends the scalability of IBM's Power Architecture in traditional embedded applications, and provides a growth platform for emerging applications such as 4G networks and WiMax infrastructure products.

The processor dissipates just 1.6 watts at these performance levels when fabricated in IBM's 45-nanometer, silicon-on-insulator (SOI) technology,

positioning the 476FP as one of the most energy efficient embedded processor cores in the industry.

The 476FP offering includes an architectural extension of IBM's CoreConnect local bus technology (PLB6), supporting coherency for multiple processors and providing a level of scalability that is ideal for customers designing families of products and focusing on software re-use. The 476FP provides a seamless performance boost to all customers currently using the PowerPC 4xx family of processor cores, maintaining IBM's long-standing practice of protecting legacy software investments.

LSI has designed a configurable level 2 (L2) memory cache that is tightly coupled to the processor, which helps the PPC476 achieve its leading performance. There are three configurations of the L2 (256K, 512K and 1M) to allow customer optimization in a given application.

The 476FP offering consists of the PowerPC 476FP, the Level 2 cache/cache controller, and PLB6, the latest architectural extension of the CoreConnect local bus architecture. Collectively, these elements enable SoC designers to easily and rapidly develop entire families of products, scaling the number of processor cores from 1 to 16 on the bus. The bus fabric on the PLB6 is capable of supporting up to eight coherent elements, giving SoC designers the flexibility to mix and match I/O masters, processors and other accelerators within the fabric.

In addition, the 3.6mm^2 size and 1.6W power dissipation of the 476FP make it a good fit for air cooled applications, and the 45nm SOI technology provides radiation tolerance needed in aerospace and defense applications.

IBM PowerPC microprocessors, embedded processors and cores are part of the IBM Power Architecture family of products, which span applications from consumer electronics to supercomputers. The IBM

Power Architecture is an open microprocessor architecture offering scalability, flexibility and customization for leading high-performance and power-saving applications.Details of the new processor core and L2 will be presented at the Linley Tech Processor Conference, Sept. 16-17 in San Jose.

The PowerPC 476FP hardcore is expected to be available to support designs starting in Oct 2009 with production in 4Q 2010. A synthesizable version is also expected in 4Q 2010.

Source: IBM