Modelling nano-worlds

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(PhysOrg.com) -- Modelling the fabrication processes for integrated circuits can slash production development time and costs by up to 40%. But as transistors, already at nano-scales, become ever smaller, researchers are modelling new worlds.
Over the past seven years, the microprocessors in everyday electronic equipment have delivered astonishing advances in speed while reducing power consumption per transistor.

That is because the scale of the transistors manufactured in high volumes for these electronic devices decreased considerably. Current research is preparing for the 32nm and 22nm nodes and even beyond.

“At these nodes many new materials and processes are introduced and the devices become so small that we cannot be sure that the concepts developed for simulating the manufacture of larger devices can be transferred directly,” says Dr Peter Pichler, a leading researcher in computer modelling of advanced manufacturing processes from the Fraunhofer Institute for Integrated Systems and Device Technology in Germany.

Computer aided design (CAD) for new technology is becoming increasingly important as transistor fabrication grows more complex and three-dimensional. Modelling in this way can save up to 40% on development costs for manufacturing technology.

The capabilities of technology CAD have been extended by Pichler and his colleagues in a major EU-funded project. The quantitative models

built by the ATOMICS project will enable breakthrough simulations and optimisation of nano-devices at the 32nm technology node and beyond.

Dopant activation and new materials for new device generations

Important developments by the ATOMICS team were made in modelling the activation or deactivation of dopants in silicon.

Dopants are impurities added in small quantities to modify semiconductors' electrical conductivity. Semiconductors such as silicon or germanium are crystalline lattices in which each atom shares electrons with four neighbours.

Replacing some atoms with atoms of other elements, such as phosphorus or arsenic that have five bonding electrons, makes extra electrons available. Because of the additional negative charges, these are called n-type (for negative). Doping with acceptor atoms such as boron, which have only three electrons available, creates "holes" that are positively charged (p-type for positive).

The performance of microprocessors depends on extremely precise methods of ion implantation for almost all doping in silicon integrated circuits. (Ion implantation is more precise, reliable and repeatable than the older thermal diffusion of deposited dopants used previously.) To dope a semiconductor wafer, a stream of ions is fired into the substrate so that the ions come to rest around a defined depth beneath the silicon surface.

"As long as ion implantation remains the standard technique for doping, especially in this context, you will need very high doping concentrations, requiring very high dose ion implantations," says Pichler. "However, ion

implantation does a lot of damage to the crystal and a damaged crystal does not give you good performance in devices."

Therefore "annealing" is used to repair implantation-induced crystal damage through the application of very high temperatures. The earliest annealing procedures were at temperatures of 900°C and above for hundreds of minutes.

Miniaturisation required a continuous reduction of the "thermal budget", which originally referred to the product of annealing time and temperature.

Annealing in today's production processes usually means a rapid increase to the peak temperature of around 1050°C followed by immediate cooling. New techniques such as "flash annealing" or non-melt laser annealing will reduce the annealing process from seconds to milliseconds.

The work undertaken by ATOMICS has also helped to define the research route to computer modelling of processes such as flash annealing, according to Pichler.

For many years, silicon dioxide has been the material of choice in field-effect transistors because of its uniformity and high interface quality. But with the 32nm process, silicon dioxide and related materials, such as nitrided oxides, are reaching their limits and new materials need to be introduced. That adds complexity to the manufacturing process.

The ATOMICS team established quantitative models for new materials. Most important is probably "strained" silicon. But also silicon-germanium alloys and advanced point-defect engineering methods were investigated.

Silicon is strained when the silicon atoms are stretched beyond their normal interatomic distance. This can be achieved by putting the layer of silicon over a substrate of silicon germanium. As the atoms in the silicon layer align with the atoms of the underlying SiGe layer, the links between the silicon atoms become stretched - or strained. Moving the atoms apart reduces the atomic forces that interfere with the movement of electrons through the transistor. They can move 70% faster through a strained silicon transistor and switch 35% faster, resulting in better chip performance and lower energy consumption.

The industry perspective

The models created by the ATOMICS team have been validated by STMicroelectronics, a globally acting manufacturer of very advanced integrated circuits. And the lessons learnt in ATOMICS are already being applied by industry. The models have been integrated into 'Sentaurus Process', the industry-leading process simulation software from Synopsys.

The ATOMICS project received funding from the ICT strand of the EU's Sixth Framework Programme for research.

More information: www.iisb.fraunhofer.de/en/arb_geb/atomics.htm

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