

TSMC Unveils First Commercial 65-Nanometer Multi-Time Programmable Non-Volatile Memory Technology

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Taiwan Semiconductor Manufacturing Company today announced the foundry segment's first functional 65-nanometer multi-time programmable (MTP) non-volatile memory (NVM) process technology.

The technology incorporates process-qualified MTP IP blocks jointly developed with Virage Logic. The new technology is the first 2.5 volt MTP process, breaking the heretofore 3.3 volt baseline barrier. It eliminates the need for an external EEPROM currently in many systems applications, thereby reducing power, area and costs while increasing data security.

Built on TSMC's 65nm Low Power (LP) process, the new MTP technology features up to 8k bits memory size that is ideal for small memory requirements associated with MP3 music downloadable digital rights management, RFID devices, fingerprint identification applications, and pre-paid cash or phone cards.

The 65nm MTP process is built up to 10 metal layers using copper low-k interconnects and nickel silicide transistor interconnects. The technology is fully logic-compatible and the NVM memory requires no additional processes or masks. Devices built using the process will support full read and program operations across temperatures ranging from - 40 °C to 125 °C, with minimum 10-year data retention at 125 °C.

“With inputs from customers’ design needs, we are convinced this 65nm process is well-suited for applications that require a small memory footprint on a leading edge manufacturing technology,” explains Jason Chen, vice president Worldwide Sales and Marketing for TSMC.

Since TSMC first announced commercial availability of its 65nm process in 2006, the company has shipped over 700,000 12-inch wafers manufactured in its Fab 12 and Fab 14. The full 65nm process node includes logic, mixed-signal, R/F, and high-density memory options and supports a broad range of computing, communications, and consumer electronics applications.

The 65nm LP process is ideal for cellular baseband, as well as portable applications and multimedia processors. The 65nm general-purpose (G) process targets graphics, networking and high-end ASIC fabrication, while the high-speed process is intended for CPU and advanced graphics processors. The 65nm LP plus G process that offers both low power and general purpose devices on the same wafer, supports wireless and portable applications requiring both low power and high performance.

TSMC’s 65nm node also supports an embedded DRAM option for high bandwidth, fast data rate designs found in high-speed consumer applications and in very small form factor handheld devices.

All TSMC 65nm processes are supported by the company’s Design Support Ecosystem featuring DFM-compliant products and services; by TSMC Reference Flow design methodology; and by a variety of process-proven TSMC and third party IP libraries including a memory compiler, I/O and standard cell libraries.

Source: TSMC

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