Smaller, cheaper cell phones possible

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(PhysOrg.com) -- Ph.D. candidate Sataporn Pornpromlikit played a critical role in research at UC San Diego that made a big impact at a recent conference, and might provide manufacturers with the means for making cell phones both smaller and cheaper.

Pornpromlikit, who goes by the name Aui (pronounced way), was the lead author on the prize-winning paper, which was based on research carried out in the Power Amplifier Lab at UC San Diego's California Institute for Telecommunications and Information Technology (Calit2). The paper outlines a new method for integrating a cell phone's power amplifier on the same chip with the rest of its internal parts using standard CMOS technology.

CMOS, or Complementary Metal Oxide Semiconductor, is a low-cost integrated circuit process technology that has been driving the communications industry for the last few decades. Although the majority of cell phone circuitry has been successfully integrated onto a single silicon chip using CMOS, until recently the power amplifier -- the part of the device that amplifies the telephone signal -- needed a separate chip because of its high voltage requirement.

"Power amplifiers are among the most power-consuming components in the transceiver and need to be designed for the best power efficiency to maximize the cell phone's battery life," explains Aui. "They also need the best signal quality and to provide the required large output power.

"With the low breakdown voltage limit allowed by the advanced CMOS

process," he adds, "the power efficiency suffers severely."

But his design solves the problem, Aui says, by distributing the required voltage equally among stacked transistors to allow for safe operation, even with the highest power output.

"With this paper, we show that it is possible to implement high-performance power amplifiers in CMOS technology while also exhibiting high power efficiency comparable to those amplifiers implemented using expensive processes."
And when the manufacturer saves money, the reduced cost theoretically trickles down to the consumer.

Aui tested his integrated circuit design on Calit2's record-setting CalHPA testbed in the Power Amplifier Lab. His paper, titled "A 33-dBm 1.9-Ghz Silicon-on-Insulator CMOS Stacked-FET Power Amplifier," won second prize in the student paper competition at the joint annual meetings in Boston of the Radio Frequency Integrated Circuits conference (RFIC 2009) and the International Microwave Symposium (IMS 2009). His co-authors included UC San Diego post-doctoral associate Calogero Presti; Antonino Scuderi of STmicroelectronics; JinHo Jeong, who is now on the faculty at South Korea's Kwangwoon University; and Peter Asbeck, a professor of electrical and computer engineering in the Jacobs School.

Calling the prize a "come-from-behind victory," Calit2 staff researcher and director of the Power Amplifier Lab, Don Kimball, explains that "the odds were stacked against them as it was a stacked MOSFET design fraught with risk." MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor, a type of field-effect transistor to amplify or switch electronic signals.

Aui hails from Bangkok and arrived at UC San Diego via MIT, where he

earned his S.B. and M.Eng degrees. He adds: "We are currently further refining our design for better performance and improved long-term reliability. With a clever tweak, we hope this technique can eventually become a risk-free design topology for any type of power amplifier."

Provided by University of California - San Diego (news : web)