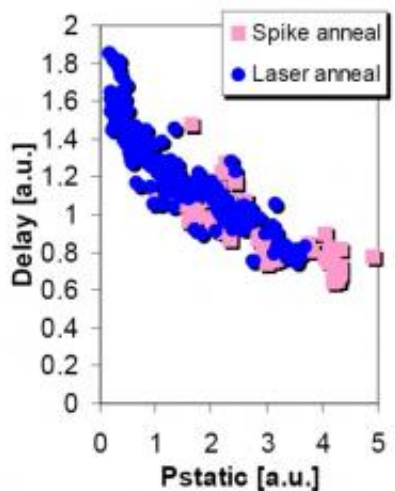


# IMEC shows optimizations for next-generation transistors

July 14 2009



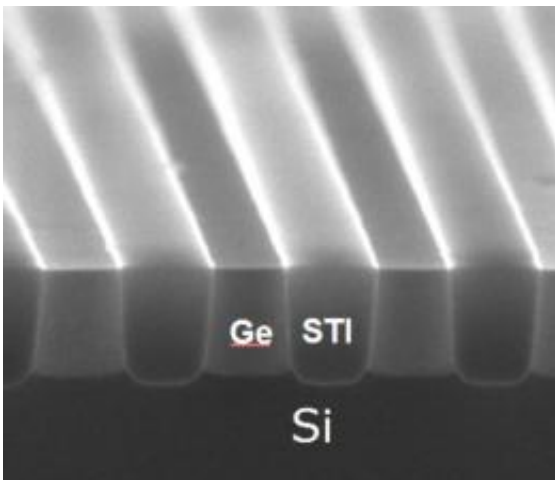
Ring oscillator delay vs. static power for spike and laser anneal.

IMEC has achieved promising results in the race to scale CMOS to 22nm and below. The breakthroughs from its transistor scaling programs include a successful integration of the laser-anneal technique in a high-K/metal-gate first process and a step forward towards fabricating aggressively scaled germanium-pFET transistors.

To scale CMOS technology to 22nm and below, high permittivity dielectrics and metal gates (Hk/MG) are considered as one of the best options. One Hk/MG integration scheme is metal inserted poly-silicon (MIPS). With a MIPS CMOS process flow, [IMEC](#) has compared spike

anneal and laser anneal. For the first time, IMEC has shown functional ring oscillators with millisecond anneal-only that show a similar performance as oscillators made using spike anneal.

The major advantage of using laser anneal over spike anneal is the reduced thermal budget. This limits the diffusion of dopants in the Si during their activation. Such a limited diffusion helps to keep short channel effects under control as the physical dimensions of the transistors shrink. But laser anneal is also challenging. IMEC's results point to optimizations of the process that limit the defects, maintain a low gate resistance, and show an excellent effective work-function control using high-K capping layers. Capping layers are dielectric layers that are deposited between the bulk dielectric and the metal gate to tune the effective work function of the [electrode](#) to the desired type (n- or p-).



X-SEM picture of the Ge-in-STI structure.

Another scaling option that has attracted a lot of attention is using high-mobility materials to boost the carrier mobility of the MOS [transistors](#),

as this can lead to higher drive currents. This search has led to an interest in [Germanium](#) MOSFETs: it has proved possible to make Ge pFET devices with a hole mobility that is substantially above the hole mobility curve of silicon, and with conventional processes. IMEC's research now shows, for the first time, an STI module (Shallow Trench Isolation) integrated in an advanced 70nm Ge-pFET technology allowing EOT in inversion scaling down to 0.85nm. IMEC has also made an in-depth analysis of the mechanisms that limit the hole mobility for sub-nm EOT Ge pFETs. These results pave the way for further optimizations of Ge pFET devices, and for their introduction in high-end high-performance ICs.

These results were obtained in cooperation with IMEC's key partners in its core programs: Intel, Micron, Panasonic, Samsung, TSMC, Elpida, Hynix, Powerchip, Infineon, NXP, Qualcomm, Sony, ST Microelectronics.

Source: IMEC

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