GaAs self-assembled nanowires could make chips smaller and faster

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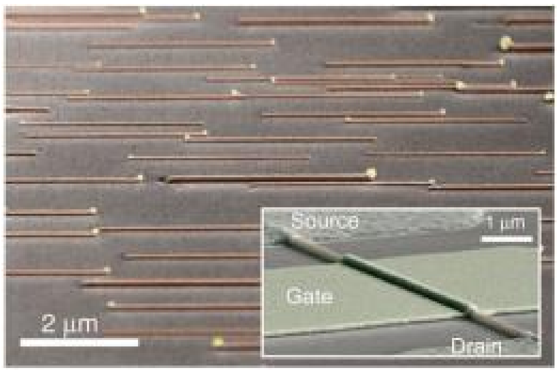

A scanning electron microscope image of self-assembled and self-aligned, planar gallium arsenide nanowires. The inset shows a field effect transistor fabricated with one of the nanowires.

(PhysOrg.com) -- Researchers at the University of Illinois have found a new way to make transistors smaller and faster. The technique uses self-assembled, self-aligned, and defect-free nanowire channels made of gallium arsenide.

In a paper to appear in the IEEE (Institute of Electrical and Electronics Engineers) journal *Electron Device Letters*, U. of I. electrical and computer engineering professor Xiuling Li and graduate research assistant Seth Fortuna describe the first metal-semiconductor field-effect transistor fabricated with a self-assembled, planar gallium-arsenide nanowire channel.

Nanowires are attractive building blocks for both electronics and photonics applications. Compound semiconductor nanowires, such as gallium arsenide, are especially desirable because of their better transport properties and versatile heterojunctions. However, a number of challenges - including integration with existing microelectronics - must first be overcome.

"Our new planar growth process creates self-aligned, defect-free gallium-arsenide nanowires that could readily be scaled up for manufacturing purposes," said Li, who also is affiliated with the university's Micro and Nanoelectronics Laboratory and the Beckman Institute. "It's a non-lithographic process that can precisely control the nanowire dimension and orientation, yet is compatible with existing circuit design and fabrication technology."

The gallium-arsenide nanowire channel used in the researchers' demonstration transistor was grown by metal organic chemical vapor deposition using gold as a catalyst. The rest of the transistor was made with conventional microfabrication techniques.

While the diameter of the transistor's nanowire channel was approximately 200 nanometers, nanowires with diameters as small as 5 nanometers can be made with the gold-catalyzed growth technique, the researchers report. The self-aligned orientation of the nanowires is determined by the crystal structure of the substrate and certain growth parameters.

In earlier work, Li and Fortuna demonstrated they could grow the nanowires and then transfer-print them on other substrates, including silicon, for heterogeneous integration. "Transferring the self-aligned planar nanowires while maintaining both their position and alignment could enable flexible electronics and photonics at a true nanometer scale," the researchers wrote in the December 2008 issue of the journal

Nano Letters.

In work presented in the current paper, the researchers grew the gallium-arsenide nanowire channel in place, instead of transferring it. In contrast to the common types of non-planar gallium arsenide nanowires, the researchers' planar nanowire was free from twin defects, which are rotational defects in the crystal structure that decrease the mobility of the charge carriers.

"By replacing the standard channel in a metal-semiconductor field-effect transistor with one of our planar nanowires, we demonstrated that the defect-free nanowire's electron mobility was indeed as high as the corresponding bulk value," Fortuna said. "The high electron mobility nanowire channel could lead to smaller, better and faster devices."

Considering their planar, self-aligned and transferable nature, the nanowire channels could help create higher performance transistors for next-generation integrated circuit applications, Li said.

The high quality planar nanowires can also be used in nano-injection lasers for use in optical communications.

The researchers are also developing new device concepts driven by further engineering of the planar one-dimensional nanostructure.

Source: University of Illinois at Urbana-Champaign (news : web)