NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs

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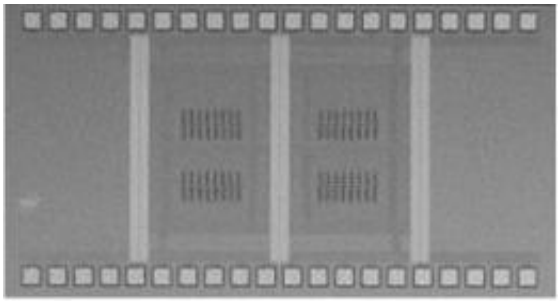

Die photo

NEC Corporation today announced that it has succeeded in demonstrating the operation of a nonvolatile magnetic flip flop (MFF).

The demonstration provides an outlook into the possibility of creating SoCs that are developed using standard tools already familiar to LSI designers, which require zero power while in a standby state, and can rapidly return to activity.

NEC's MFF operations were produced by integrating data flip flop (DFF) with magnetic tunnel junctions (MTJ), in addition to circuits that switch the direction of MTJ's magnetization. Please see below for more detail on MFF features.

1.The MFF operates on the same voltage as existing flip flops, which

enables its versatile use as a library tool for automatic layout design of SoCs.

2. During normal operation, the MFF is designed to prevent MTJs from affecting MFF clock frequency, as it can operate at the same 3.5 GHz as DFF.

3. In the event of a sudden power failure, the MTJs may carry out MFF functions.

The MTJs in the MFF were created using the same process as the MTJs in the 250-MHz high speed MRAM that was originally developed, designed and fabricated by NEC, and features MTJ layers being incorporated into an inter-metal oxide layer. The process makes it easy for both MFFs and MRAMs to be integrated into one SoC.

SoC power consumption tends to increase in relation to miniaturization and greater circuit sophistication. However, the demand for electronic appliances that use SoCs and consume low power is steadily increasing. It has now become an essential task for electronic appliance development to address the need for both advanced functions and low power consumption. The development of mobile appliances powered by batteries is particularly influenced in consideration of their need to reduce power consumption in both standby and operation mode.

In order to reduce SoC power consumption, one effective method is to eliminate the need for power when the SoC is inactive. However, SoC logic circuits consist of CMOS gates whose data may be lost by removing power. Since important data must be protected even in standby mode, the power supply to some portions of the SoC cannot be cut. Therefore, it is difficult to reduce standby current for an SoC to zero.

Since logic circuits in almost all SoCs consist of clock synchronized

circuits, when a DFF becomes nonvolatile, all logic circuits can become nonvolatile. If DFFs are replaced with MFFs and volatile SRAMs are replaced with nonvolatile MRAMs, an SoC can become nonvolatile, which facilitates the design of standby-power-free SoCs.

The FeRAM technology that removes volatility from DFFs has already been in use, but its implementation was confined due to limited write cycles. Furthermore, although the latest SoC operate at 1.2 V or the less, the voltage is too low for ferro-electronic elements of FeRAM to be controlled. Therefore, it is difficult for FeRAM based nonvolatile flip flop DFF to be used as a library tool for automatic layout design of SoCs.

This successful MFF demonstration, however, provides insight into how the above issues can be solved by using MFFs and MRAMs that require 1.2 V or less and have unlimited write endurance. Looking forward, NEC will continue developing original technologies that apply MTJ to SoCs, as the company also aims to demonstrate an SoC integrated with MFFs.

Provided by NEC