Toshiba, IBM, AMD Develop World's Smallest FinFET SRAM Cell with High-k/Metal Gate

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Toshiba, IBM, and AMD today announced that they have together developed a Static Random Access Memory (SRAM) cell that has an area of only 0.128 square micrometers (μm^2), the world's smallest functional SRAM cell that makes use of fin-shaped Field Effect Transistors (FinFETs).

The cell, developed with a high-k/metal gate (HKMG) material, offers advantages over planar-FET cells for future technology generations. SRAM cells are circuit components in most systems-level, large-scale integrated circuits such as microprocessors, and smaller SRAM cells can help provide smaller, faster processors that consume less power. The technology was announced on December 16 in a technical paper presented at the 2008 International Electron Devices Meeting in San Francisco, California.

To reduce the transistor size when SRAM cells are created using conventional planar transistors, IC manufacturers generally adjust properties by doping more impurities into the device area. However, this adjustment creates undesirable variability and deteriorates the SRAM stability. This issue is becoming critical, especially at the 22nm technology node and beyond. The use of FinFETs -- vertical transistors with fin-shaped undoped silicon channels -- is an alternative approach to allow SRAM cell size reduction with less characteristic variation.

Researchers from the three companies fabricated a highly scaled FinFET SRAM cell using HKMG. It is the smallest nonplanar-FET SRAM cell yet achieved: at 0.128μm^2, the integrated cell is more than 50 percent smaller than the 0.274μm^2 nonplanar-FET cell previously reported. To achieve this goal, the team optimized the processes, especially for depositing and removing materials, including HKMG from vertical surfaces of the non-planar FinFET structure.

The researchers also investigated the stochastic variation of FinFET properties within the highly scaled SRAM cells and simulated SRAM cell variations at an even smaller cell size. They verified that FinFETs without channel doping improved transistor characteristic variability by more than 28 percent. In simulations of SRAM cells of 0.063μm^2 area, equivalent to or beyond the cell scaling for the 22nm node, the results confirmed that the FinFET SRAM cell is expected to offer a significant advantage in stable operation compared to a planar-FET SRAM cell at this generation.

By successfully fabricating highly scaled FinFET SRAM cells with HKMG, the companies have positioned FinFETs as an attractive transistor structure for SRAMs in the 22nm node and beyond. The new technology is a step forward to more powerful practical devices.

Provided by IBM