IBM Develops Computational Scaling Solution for Next Generation '22nm' Semiconductors

September 17 2008

In response to ever increasing demands for smaller, more powerful and energy-efficient devices for cloud computing and high-performance servers, IBM today announced the semiconductor industry's first computationally based process for production of next generation 22nm semiconductors. Known as Computational Scaling (CS) -- a process that enables the production of complex, powerful and energy-efficient semiconductors at 22nms and beyond -- this new initiative will feature support from several of IBM's key partners initially including Mentor Graphics and Toppan Printing.

Today, most integrated circuits are manufactured at 45nm or larger technology nodes. Producing circuits at 22nm is a challenging milestone since current lithography methods -- the process of designing photomasks to image circuit patterns on silicon wafers in mass quantity -- are not adequate for critical layers at 22nm due to fundamental physical limitations. Computational Scaling overcomes these limitations by using mathematical techniques to modify the shape of the masks and characteristics of the illuminating source at each layer of an integrated circuit.

This initiative directly links to IBM's Cloud Computing strategy, which offers highly scalable, more energy efficient Web services. Through cloud computing, enterprises and individuals can access these services in a highly flexible and open environment. As demand for these services

grows, more powerful and flexible servers based upon advanced technologies will be required.

"The traditional scaling approach is optical-resolution centric," said Gary Patton, vice president, IBM Semiconductor Research and Development Center. "IBM's Computational Scaling approach is centered on advanced mathematical techniques encapsulated in software tools that use high performance computing systems. This technique also makes technology complexity transparent to the designer and maximizes flexibility through integrated flows and automation."

IBM's CS solution is an ecosystem that includes the following components: a new resolution enhancement technique (RET) that uses source-mask optimization (SMO); virtual silicon processing with TCAD; predictive process modeling; design-rule generation and corresponding models; design tooling; design enablement; complex illumination; variance control; and mask fabrication, along with necessary partnerships.

The strategy of combining the strengths of industry leading partners for CS will leverage IBM's core strengths in successful management of innovative partnerships, semiconductor processing, high performance computing, IC design, design tooling and system integration.

The individual components of IBM's CS solution include:

Source Mask Optimization
IBM has partnered with Mentor Graphics on a new resolution enhancement technique to enable cost-effective printing of two dimensional patterns for the 22nm semiconductor technology generation. This new technology, know as source mask optimization, will provide a means to minimize the use of double patterning by employing highly customized sources with optimized mask shapes.

"Our partnership with IBM will ensure production-ready technologies are in place when they are needed for the 22nm node," said Joseph Sawicki, vice president and general manager for the design-to-silicon division at Mentor Graphics. "Because this next generation solution will be built on the familiar Calibre platform, designers will see a smooth transition path to 22nm, and will also enjoy added benefits in managing turnaround time and the cost of computing."

Virtual Fabricator
Together with Rensselaer Polytechnic Institute and the State of New York, IBM has made significant investments in the area of high performance computing and remains devoted to the advancement of semiconductor technology through the establishment of the Computational Center for Nanotechnology Innovations (CCNI). CCNI provides the unprecedented computational power to enable accurate predictions of advanced manufacturing processes. When combined with predictive models and TCAD, this platform will allow virtual co-optimization of semiconductor unit processes and critical circuit design elements to cut development learning cycles and improve time-to-market for advanced semiconductor technology.

Design Technology Co-Optimization
Within semiconductor fabrication, design 'rules' are created as an abstract representation of the information or model that describes the technology being created. Often, these rules are only defined after an exhaustive negotiation process between the technology and design team. To improve the timeliness and certainty of this process, IBM's Design Technology Co-optimization (DTCO) process helps integrate and automate this complex procedure, cutting the time it takes to reach a clear and stable set of rules for use by the circuit design teams.

Design Enablement Tools
As a result of using IBM's DTCO, a semiconductor modeling process

will have a new class of design rules that are simpler and more prescriptive (what to do vs. what not to do). Working with engineering design automation (EDA) suppliers, IBM will be providing new design enablement solutions for a seamless transition.

Critical Dimension Variance Control
Working with leading equipment suppliers, IBM will play the role of lead integrator of providing an adaptive control system to minimize critical dimension variance. As a result production yield and circuit parameters will be more stable reducing the cost of production.

Photomask Fabrication
To address the gap in raw optical resolution, aggressive resolution enhancement techniques such as SMO drive unprecedented minimum feature sizes on the photomask -- the opaque plate with holes or transparencies that allow light to shine through in a defined guide for casting the circuit patterns. IBM has partnered with Toppan to ensure timely availability of masks with the required feature sizes.

"It has been more than three years since Toppan and IBM launched our joint development project for advanced photomask process," said Toshiro Masuda, managing director and head of Semiconductor Solutions Division of Toppan Printing. "We believe our ongoing engineering collaboration will significantly enhance the success of IBM's computational scaling solution."

Provided by IBM

Citation: IBM Develops Computational Scaling Solution for Next Generation '22nm' Semiconductors (2008, September 17) retrieved 24 April 2024 from https://phys.org/news/2008-09-ibm-scaling-solution-22nm-semiconductors.html

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.