Researchers redefine ultrathin display process

July 29 2008

(PhysOrg.com) -- The Flexible Display Center at Arizona State University has developed a new process for manufacturing high-performance flexible displays on transparent plastic.

FDC researchers, working with industrial partners DuPont Teijin Films and E Ink Corp., have developed a method for making high-performance amorphous silicon thin film transistors on planarized Teonex® PEN films. The FDC team integrated 3.8-in. QVGA arrays of these transistors with Vizplex-100™ imaging layer film from E Ink to fabricate glass-free high-performance flexible electrophoretic displays that are only 15 mils (375 micrometers) thick.

The displays are quite rugged and readily withstand severe vibration and impact tests performed at industry partner General Dynamics' labs. To download video highlights of these tests go to flexdisplay.asu.edu/Flex-display-test_revB.wmv .

The FDC process uses a proprietary technique for temporarily bonding the planarized Teonex PEN film (from DuPont Teijin) to a rigid carrier using a specially developed adhesive. Amorphous silicon circuits then are fabricated with conventional flat panel display manufacturing equipment. Despite exposure of the bonded film to temperatures as high as 200 C (392 F) during the fabrication process, essentially no plastic substrate distortion is observed. The film bearing the completed transistor arrays is removed from the carrier using a mechanical force that is gentle enough to permit automation of the process.

“Most of the technology development in our pilot line environment is realized through steady improvements over several cycles of learning,” said Greg Raupp, director of FDC. “In this case, integrated learning came together as we viewed the entire flexible substrate system of carrier, adhesive, substrate, planarization and associated process protocols to point to a directed solution that yielded a dramatic technical advance.”

The FDC thin film transistors are produced using the highest semiconductor and gate-dielectric deposition temperatures reported for a process on Teonex PEN. The higher temperatures permit the fabrication of transistors with higher on-off ratio, better sub-threshold slope, and – most importantly – greater bias-stress stability. These performance characteristics translate directly into higher pixel densities for enhanced display resolution and an enlarged number of grey levels for improved image quality.

The ability to produce high quality arrays of thin film transistors with low defects is aided by the use of DTF’s planarized Teonex PEN, which has been developed to meet the needs of demanding display applications. The temporarily bonded Teonex PEN with its newly developed planarization coating provides a surface smooth enough and sufficiently defect-free to enable the fabrication of micrometer-scale electronics.

Development of methods for the handling of mechanically flexible substrates such as Teonex PEN in automated manufacturing equipment has been a significant challenge to creating practical and economical processes for flexible displays and electronics. The FDC advance in temporarily bonding plastic films to a carrier is a significant move forward for advancing engineering prototypes of flexible displays to commercial manufacturing.

Provided by Arizona State University