Engineers show nanotube circuits can be made en masse

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Most innovations don't go far unless there is a way to turn them into products that are manufacturable on a mass scale. That's why new research on carbon nanotubes, presented June 19 by a group of Stanford electrical engineers, is likely to draw industry attention.

The engineers unveiled a method for making integrated circuit chips with complex nanotube components on the scale and with the parallelism that the semiconductor industry must employ to make chips that are economical.

"We have shown here processes that are scalable, that are akin to conventional semiconductor manufacturing on the wafer scale," said electrical engineering Professor H.-S. Philip Wong, one of the authors of a paper presented at the Symposia on VLSI Technology and Circuits in Honolulu. Wafers are the large discs of silicon on which semiconductor manufacturers pattern several hundred computer chips that are then cut out and packaged as products. "The lithography is on a wafer scale, the nanotube growth is on the wafer scale and all the processes that we use here are very similar to conventional semiconductor manufacturing," Wong said.

Because of their potential to act as high-performance transistors at higher speeds and lower power than conventional silicon technology, nanotubes are the subject of intensive research worldwide. So far, however, researchers have only been able to make nanotube circuits one at a time, rather than on the scale known as VLSI, for Very Large Scale

Integration.

Moreover, the information processing components of the circuits, known as logic gates, have typically been simple inverters, rather than the whole variety of more complex gates that are needed in useful logic circuits. This new ability to make chips on a large scale with the needed variety of logic gates therefore represents an important advance toward making commercially viable nanotube integrated circuits, said Subhasish Mitra, an assistant professor of electrical engineering and of computer science.

The paper also represents the first real demonstration of a design technique that makes complex logic functional even when the nanotubes turn out to have goofy kinks and bends (rather than lying straight) or are in the wrong place. Wong and Mitra unveiled the technique last year in simulations but have now shown that it works in an actual fabrication process.

In addition to Wong and Mitra, the paper's other authors are Nishant Patil and Albert Lin, both electrical engineering graduate students, and Edward Myers, a staff member of the Stanford Nanofabrication Facility, a research fabrication facility on campus that is part of the National Nanotechnology Infrastructure Network.

Handling the heat

The Stanford-devised process involves growing nanotubes on a quartz wafer—a 4-inch diameter platter—and then transferring them like a kid's temporary tattoo onto a silicon wafer patterned with metal electrodes. The nanotubes could then connect the electrodes to make transistors and logic gates. The quartz-to-silicon transfer technology had already been established for small pieces of substrates, but what has often stymied researchers has been finding a way to grow nanotubes on such a large slab of quartz. Quartz helps facilitate nanotube growth but is

sensitive to the heat required in the process.

The Stanford engineers overcame that problem by realizing that the quartz wafer would shatter like glass if it were heated too quickly as the temperature approached a certain critical point (roughly 1,100 degrees Fahrenheit). By slowing down the heating process, the researchers kept the wafers intact.

The nanotubes were then transferred to the silicon wafer to be overlaid on the electrodes. The electrodes were patterned according to special algorithms designed to ensure that however the individual nanotubes were laid out, the logic gates that were created would still work.

In all, the group created about 197 dies, or chips, on the 4-inch diameter wafer. Each chip had about 1,000 transistors, meaning that the wafer had more than 100,000 transistors. Random testing of 18 transistors per chip revealed that 99 percent of the transistors were functional. Full-scale commercial chips, of course, would require millions of transistors per chip and sophisticated interconnections among them.

Even before a full-fledged commercial nanotube chip could be designed, more research is needed to resolve some fundamental problems. Among them is a need to increase the density of nanotubes on the wafer, a goal that could be accomplished by repeated transfers from different quartz wafers to the same silicon wafer and further optimizing the nanotube growth conditions. In addition, researchers must find a way to thoroughly weed from their logic gates pesky "metallic" nanotubes, which can short-circuit transistors.

Still, the researchers are optimistic about the progress so far.

"The fundamental problem in this domain which we were able to overcome is that in the past researchers would have to find the nanotubes

on the substrate and then make devices and circuits wherever they were," Mitra said. "But you want to be able to make things in parallel—at VLSI scale—without worrying about the exact placement and orientation of the nanotubes. We can now show that we are able to do that."

Source: Stanford University