New technique to optimize computer speed

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Who doesn't dream of increasingly fast computers that consume less and less energy? To design these computers of the future, it is important to be able to control nanoscale strain in the processors. Until now, this strain remained difficult to observe. Now, thanks to a new electron holography technique invented by researchers at the Centre d'élaboration de matériaux et d'études structurales (CEMES-CNRS), it is possible to map deformation in a crystal lattice with a precision and resolution never previously attained.

This new patented measurement device overcomes nearly all the limitations of current methods. It should enable manufacturers to

improve microprocessor production methods and to optimize future computers. This work is published in the June 19, 2008 issue of the journal Nature.

“Strained” silicon is a fundamental component of all recent microprocessors. The reason for its success is that local strain-induced deformation in the crystal lattice improves processor performance. The deformation significantly increases electron mobility, making it possible to boost computer speed and reduce energy consumption. However, since manufacturers could not analyze deformation accurately, they didn’t have complete mastery of chip design. They essentially relied on simulations and monitoring of performance without ever truly knowing the strain state. This problem has now been resolved, thanks to a new strain measurement method developed by a CNRS team in Toulouse.

Based on electron holography, the technique certainly has appeal: it makes it possible to measure deformation (compression, tension, and shear strain) in numerous materials with high precision and spatial resolution. Precision exceeds 0.1%, or 0.5 picometers (2) and spatial resolution is on the nanometer scale. But the real innovation compared to traditional techniques is that it is makes it possible to analyze larger areas (a micrometer rather than the previous 100 nanometers) with a level of precision never reached before.

This measurement technique offers further advantages. It makes it possible to study samples that are ten times thicker than previous samples (300 nm), which guarantees that observations are accurate. The thicker the sample, the less the strain is relaxed, and the closer the measured stain is to that of a real system. In addition, the measurements are taken directly, unlike other techniques that require a certain number of preliminary simulations.

This technique, patented by CNRS in September 2007, will in all

likelihood become the leading method for measuring crystal lattice strain at the nanometer scale. It will optimize strain modeling in transistors and enhance their electrical efficiency.

Source: CNRS