Microchip sets low-power record with extreme sleep mode

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A low-power microchip developed at the University of Michigan uses 30,000 times less power in sleep mode and 10 times less in active mode than comparable chips now on the market.

The Phoenix Processor, which sets a low-power record, is intended for use in cutting-edge sensor-based devices such as medical implants, environment monitors or surveillance equipment.

The chip consumes just 30 picowatts during sleep mode. A picowatt is one-trillionth of a watt. Theoretically, the energy stored in a watch battery would be enough to run the Phoenix for 263 years.

Scott Hanson, a doctoral student in the U-M Department of Electrical Engineering and Computer Science, will present the design June 20 at the Institute of Electrical and Electronics Engineers' Symposium on VLSI Circuits. Hanson jointly leads this project with Mingoo Seok, a doctoral student in the same department.

Phoenix measures one square millimeter. There's nothing special about its size, as chips in many modern sensors and electronics are one square millimeter and smaller. But Phoenix is the same size as its thin-film battery, marking a major achievement.

In most cases, batteries are much larger than the processors they power, drastically expanding the size and cost of the entire system, said David Blaauw, a professor in the Department of Electrical Engineering and

Computer Science. For instance, the battery in a laptop computer is about 5,000 times larger than the processor and it provides only a few hours of power.

"Low power consumption allows us to reduce battery size and thereby overall system size. Our system, including the battery, is projected to be 1,000 times smaller than the smallest known sensing system today," Blaauw said. "It could allow for a host of new sensor applications."

A group of U-M researchers is putting the Phoenix in a biomedical sensor to monitor eye pressure in glaucoma patients. Engineers envision that chips like this could also be sprinkled around to make a nearly invisible sensor network to monitor air or water or detect movement. They could be mixed into concrete to sense the structural integrity of new buildings and bridges. And they could power a robust pacemaker that could take more detailed readings of a patient's health, researchers say.

To achieve such low power, Phoenix engineers focused on sleep mode, where sensors can spend more than 99 percent of their lives. Sensors wake only briefly to compute at regular intervals.

"Sleep mode power dominates in sensors, so we designed this device from the ground up with an efficient sleep mode as the No. 1 goal. That's not been done before," said Dennis Sylvester, an associate professor in the Department of Electrical Engineering and Computer Science.

The system defaults to sleep. A low-power timer acts as an alarm clock on perpetual snooze, waking Phoenix every ten minutes for 1/10th of a second to run a set of 2,000 instructions. The list includes checking the sensor for new data, processing it, compressing it into a sort of short-hand, and storing it before going back to sleep.

The timer "isn't an atomic clock," Hanson said. "We keep time to 10 minutes plus or minus a few tenths of a second. For the applications this is designed for, that's okay. You don't need absolute accuracy in a sensor. We've traded that for enormous power savings."

A unique power gate design is an important part of the sleep strategy. Power gates block the electric current from parts of a chip not essential for memory during sleep.

In typical state-of-the-art chips, power gates are wide with low resistance to let through as much electric current as possible when the device is turned on. These chips wake up quickly and run fast, but a significant amount of electric current leaks through in sleep mode.

Phoenix engineers used much narrower power gates that restrict the flow of electric current. That strategy, coupled with the deliberate use of an older process technology, cut down on energy leaks.

"A power gate of such a small size is unheard of in traditional design since it severely limits the performance of the chip," Seok said.

To address this performance loss, the Michigan team increased the chip's operating voltage, increasing the baseline power by approximately 20 percent when the chip is awake. But Phoenix still runs at 0.5 Volts, rather than the 1 to 1.2 Volts typical chips require.

Source: University of Michigan