Novel memory device is set to rival transistor-switched silicon-based memory

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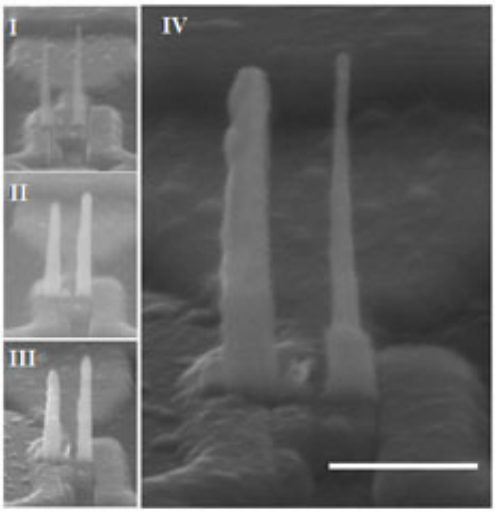

NEM switch fabrication steps. I. Metallic multi-walled nanotubes are grown from catalyst dots defined by electron-beam lithography. II. The nanotubes are coated with an insulating layer of silicon nitride. III. Chromium is sputtered to form the capacitor on the source electrode. IV. A wet etch exposes the nanotube on the drain electrode, which is the moving part of the switch.

Working with an international group of researchers, Professor Gehan Amaratunga has produced a novel memory device which is set to rival transistor-switched silicon-based memory.

In the world of technology, expanding knowledge results in shrinking products. Laptops, mobile phones and MP3 players are as small as their

components allow. Companies are constantly battling to make their products faster, smarter and smaller. Conventional memory chips in electronic devices are made up of transistors, resistors, and capacitors built in layers on a silicon wafer through a photolithographic process, during which precise patterns are etched on the silicon to form the chip. Today's technology allows several million transistors to be built on a piece of silicon the size of a pinhead, but many researchers believe this form of memory has been pushed to its limits.

In computing, information is stored in bits which can have one of two possible values or states: 1/ON or 0/OFF. The most common type of memory in use today is volatile random-access memory (volatile RAM) which requires a power source to store data. Volatile RAM may be divided into two types: dynamic and static (DRAM and SRAM). In DRAM each memory cell can consist simply of one capacitor and one transistor. The capacitor holds the bit of information, the transistor acts as a switch, letting the control circuitry on the chip read the capacitor or change its state (e.g. from ON to OFF). Reading the state of the capacitor destroys the information in it and so the read operation must be followed by a write operation in which the state of the capacitor is restored. The capacitor consists of two charged layers separated by an insulator. The capacitor leaks charge and the information eventually fades unless the capacitor charge is refreshed. The thinner insulators get the more they allow charges to tunnel through.

The second type of volatile RAM, SRAM does not need to be periodically refreshed and so has significantly faster access times than DRAM. It also requires less power in operation. However, six transistors are required to form a single SRAM cell. Although inferior to SRAM, DRAM is used because the small number of components required means that a cell can occupy less area on a silicon chip. Another factor affecting the area a cell requires is the size of the components themselves. Decreasing component sizes and increasing silicon wafer

sizes are the major factors in driving down the cost of silicon devices. However, it is becoming increasingly difficult to achieve reduced feature sizes in the manufacturing process. Complex and expensive fabrication techniques have been developed to keep pace with the demand for cheaper and faster silicon-based memory.

Researchers have been trying to create electromechanically driven switches small enough to rival transistor-switched silicon-based memory. Unlike transistors, electromechanically driven switches contain moving parts. Not only do electromechanical devices have excellent ON-OFF ratios and fast switching characteristics, but the physical separation between the switch and the capacitor in such devices means the data leakage problem is significantly reduced. However, until now the technology has not been a viable alternative to silicon-based arrangements because it involved larger cells and more complex fabrication processes.

Professor Amaratunga and his team have remedied these drawbacks by creating a novel nanoelectromechanical (NEM) switched capacitor based on vertically aligned multiwalled carbon nanotubes (CNTs). Rather than creating memory chips through a photolithographic process, nanotubes are grown in place on a silicon wafer by allowing a carbon-carrying gas to absorb onto a hot nickel surface, which acts as a catalyst for the nanotube growth. The length of time for which the nanotube is grown determines its length, which in turn determines its mechanical properties such as stiffness and resonant frequency. The resonant frequency of the nanotube structure determines the maximum switching speed of the NEM switch and its stiffness determines how much charge is needed to deflect it into contact with the other element of the cell.

One nanotube which stores an electric charge bends toward a static nanotube. When the two touch, an electrical contact is created and charge can flow to a capacitor structure formed around the static

nanotube. This charge is used to represent a bit of information; a charged capacitor represents 1/ON and an uncharged capacitor represents 0/OFF. The vertical nature of the NEM capacitor structure allows for high integration densities, reducing both process costs and size requirements. There is a sharp transition between the ON and the OFF state of the switch which means that a very small difference in voltage can change the state of the device, reducing the amount of power required for its operation.

Nanoelectromechanical devices based on carbon nanotubes have been reported previously, but this is the first time researchers have been able to control the number and spatial location of nanotubes over large areas with the precision needed for the production of integrated circuits.

These results have been reported in a paper in the December 23, 2007 online edition of Nature Nanotechnology: "Nanoscale memory cell based on a nanoelectromechanical switched capacitor".
www.nature.com/nnano/journal/v … /nnano.2007.417.html

Source: the University of Cambridge