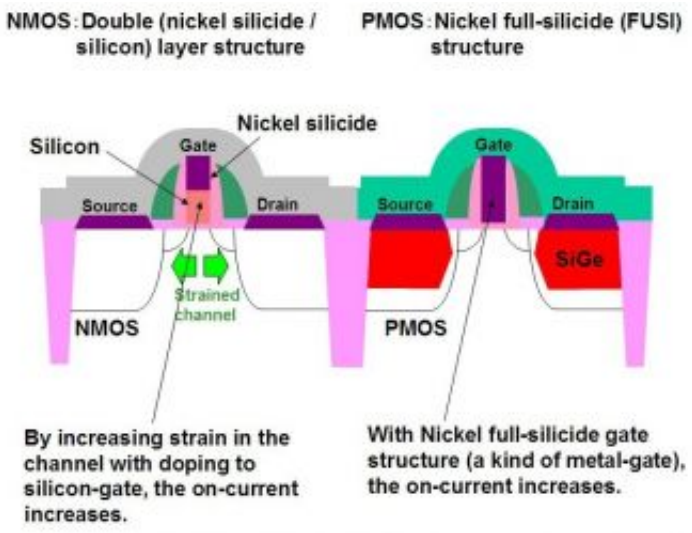
Fujitsu Develops Low-power CMOS Technology For 32nm Generation

June 17 2008



32nm-generation low-power CMOS technology

Fujitsu today announced the development of low-power CMOS technology for 32nm-generation logic LSIs, which makes it possible to minimize the number of necessary manufacturing processes for LSIs, and without the need to utilize additional new materials.

While minimizing rising costs associated with a rise in additional manufacturing processes, the newly developed technology can reduce power-supply voltage without causing a drop in operation speeds, and can lower operational power consumption by approximately 40% compared to technologies for 45nm-generation logic LSIs.

It is anticipated that this new technology can be used for wide range of applications, such as for system LSIs for mobile devices which are becoming increasingly multi-functional, and microprocessors that are increasingly adopting multi-core configurations.

Details of this technology will be presented at the 2008 Symposium on VLSI Technology, to be held from June 17 to June 19 in Honolulu, Hawaii.

Reducing power-supply voltage is an effective means of reducing power consumption in NMOS and PMOS transistors, the basic devices of logic LSIs. However, simply lowering power-supply voltage decreases the on-current that a MOS transistor can supply, thus leading to a drop in operation speed. In response to this problem, it is expected that various companies are planning to use metal for gate electrode material as a promising alternative to a conventional silicide/silicon structure, with the aim of achieving high speed and low power consumption in 32nm logic LSIs which are slated for deployment around 2010. A metal gate electrode can significantly increase the on-current that a MOS transistor can supply, thereby enabling a logic LSI to consume less power without degrading operating speed.

With metal gate electrodes for 32nm-generation logic LSIs, to achieve on-current equivalent to that of previous levels even while using low voltage, NMOS and PMOS devices must have different metal materials for their gate electrode, thus leading to a rise in costs due to the necessitation of new materials and the need for additional manufacturing processes.

By developing new technology for both NMOS and PMOS devices, and by minimizing the need for new materials or an increase in additional manufacturing processes, Fujitsu Laboratories succeeded in lowering power consumption without degrading operating speed, on par with

other 32nm metal gate technologies reported thus far.

Key features of the new technology are:

1. Double-layer gate technology for NMOS
For the NMOS device, the new technology uses a conventional double-layer gate-electrode structure consisting of a nickel-silicide layer and a silicon layer, but adds impurities to the silicon layer. This adds a large amount of strain to the channel region where on-current flows thereby increasing the on-current. As a result, the device can be operated with less power without degrading operating speed.

2. Nickel fully silicided gate technology for PMOS
By employing high-temperature heat treatment and optimized structures, the technology makes it possible to fully silicide just the PMOS gate electrode, by using nickel which has been widely used in the past as a silicide material. Because this gate electrode based on nickel silicide functions as a metal gate electrode, there are no remarkable drops in performance due to depletion in the gate electrode - a common problem for conventional silicide/silicon gate PMOS in particular - and as a result, on-current can be increased. Thus, this PMOS nickel fully-silicided gate technology enables low-power operation without degradation of operation speeds compared to 45nm logic LSIs.

By utilizing this new technology, it was possible to significantly reduce the number of necessary new manufacturing process from six to just one process, compared to 32nm-generation metal gate technologies that were previously reported. As a result, cost increase was limited to less than 1% technology in comparison with other 32nm metal gate technology.

In terms of performance, on par with other 32nm metal gate technologies, the new technology can lower power-supply voltage without a drop in operating speed compared to 45nm logic LSIs and thus

reduces operational power consumption by approximately 40%.

Source: Fujitsu