Nano-designed transistors with disordered materials, but high performance

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The Holy Grail for transistor designers has been the requirement to be able to get high performance at reduced costs over very large substrate areas. Transistors on cheap and flexible substrates like glass and plastics are currently unable to deliver such performance and therefore do not lend themselves to seamless monolithic integration of increased electronic functions on human interface devices (displays and sensors).

At present, high performance transistors are only available in crystalline materials which are expensive and have to be attached ex-situ onto larger area substrates, which adds to the expense and complexity of system design. If both the electronics and display substrates can be integrated onto one platform, it would usher a new dawn in immersive and personal electronics.

Individuals will thus be able to communicate, send and receive information of value, and access data about their current environment and health status with freedom, at leisure, and in comfort.

However, in general, the deposition of semiconductor films used to make transistors on such substrates has to be carried out at low temperatures to preserve substrate integrity. As a result, the quality of the organic or inorganic semiconductor films is severely constrained, and has a dramatic influence on the transistor performance.

In a recent report to be published in *Science – 'Engineering Perspectives'*, backed by a further paper to appear in *IEEE Electron Device Letters*,

engineers propose the use of clever transistor structure designs to overcome some of the issues with obtaining suitably low power and high speed operations in standard material systems.

In the first collaborative work with Hitachi Central Research Laboratory, Japan, researchers at the Advanced Technology Institute of the University of Surrey have experimentally and theoretically demonstrated that for transistors of disordered silicon films, superior switching performance (low leakage current, and steep sub-threshold slope) can be achieved by making the conduction channel in the transistor very thin.

A higher $I_{ON/IOFF}$ ratio, which exceeds 10^{11}, can be achieved for devices with a 2.0-nm-thick channel. Another seminal work from the same research laboratory at Surrey, is on the newly developed source-gated transistor (SGT) concept by Professor John Shannon. Compared to a field-effect transistor, the SGTs can operate with very short source–drain separations even with a thick gate insulator layer to achieve high speed, good stability and superior control of current uniformity, providing a significant advantage in terms of the fabrication process.

Dr Xiaojun Guo, one of the lead investigators, comments: "Engineering of the transistor structure itself rather than the channel material can lead to improved device performance. It will enable the design of high-performance large area circuits and systems based on low-cost reliable material processes".

Professor Ravi Silva, Director of the Advanced Technology Institute states: "This work will help extend the already well established CMOS fabrication technologies for use in large area applications such as displays and sensors, which are at the heart of consumer electronics. The ATI is fortunate that we have been at the forefront of two potential technologies that can lead to enhanced device performance in disordered materials by clever nano-scale structural design of disordered transistors.

This type of work sponsored by the EPSRC forms the bedrock for future electronic technologies".

This research will be published in the journal 'Science', and a more detailed version of the nano-designed transistor will appear in 'IEEE Electron Device Letters'.

References cited:

1. X. Guo and S.R.P. Silva, 'High-Performance Transistors by Design', *Science*, vol 320, 02 May 2008

2. X. Guo, T. Ishii, and S.R.P. Silva, 'Improving Switching Performance of Thin-Film Transistors in Disordered Silicon', to appear in *IEEE Electron Device Letters*, vol 29 Issue 6, 2008.

Source: University of Surrey