

Intel, STMicroelectronics Deliver Industry's First Phase Change Memory Prototypes

February 6 2008

Intel Corporation and STMicroelectronics reached a key industry milestone today as they began shipping prototype samples of a future product using a new, innovative memory technology called Phase Change Memory (PCM). The prototypes are the first functional silicon to be delivered to customers for evaluation, bringing the technology one step closer to adoption.

The memory device, codenamed "Alverstone" uses PCM, a promising new memory technology providing very fast read and write speeds at lower power than conventional flash, and allows for bit alterability normally seen in RAM. PCM has long been a topic of discussion for research and development, and with "Alverstone," Intel and STMicroelectronics are helping to move the technology into the marketplace.

"This is the most significant non-volatile memory advancement in 40 years," said Ed Doller, chief technology officer-designate of Numonyx, the new name for the pending STMicroelectronics and Intel flash memory company. "There have been plenty of attempts to find and develop new non-volatile memory technologies, yet of all the concepts, PCM provides the most compelling solution – and Intel and STMicroelectronics are delivering PCM into the hands of customers today. This is an important milestone for the industry and for our companies."

In related news, Intel and STMicroelectronics technologists presented a



research paper this week at the International Solid States Circuits Conference (ISSCC) describing yet another breakthrough in PCM technology. Together, the companies created the world's first demonstrable high-density, multi-level cell (MLC) large memory device using PCM technology. The move from single bit per cell to MLC also brings significantly higher density at a lower cost per Mbyte making the combination of MLC and PCM a powerful development.

In 2003, Intel and STMicroelectronics formed a joint development program (JDP) to focus on Phase Change Memory development. Previously the JDP demonstrated 8Mb memory arrays on 180nm at the 2004 VLSI conference and first disclosed the Alverstone 90nm 128Mbit memory device at the 2006 VLSI Symposium. Alverstone and future JDP products will become part of Numonyx, a new independent semiconductor company created through an agreement between STMicroelectronics, Intel and Francisco Partners signed in May 2007. The new company's strategic focus will be on supplying complete memory solutions for a variety of consumer and industrial devices, including cellular phones, MP3 players, digital cameras, computers and other high-tech equipment. The companies are scheduled to close the transaction in the first quarter of 2008.

In 2007, the combined memory market for DRAM, flash, and other memory products such as EEPROM was US\$61 billion, according to the industry research firm Web-Feet Research, Inc. Memory technology cost declines have traditionally been driven at the rate of "Moore's Law," where density doubles every 18 months with each lithography shrink. As RAM and flash technologies run into scaling limitations over the next decade, PCM costs will decline at a faster rate. The advent of multi-levelcell PCM will further accelerate the cost per bit crossover of PCM technology relative to today's technologies. Finally, by combining the bitalterability of DRAM, the non-volatility of flash, the fast reads of NOR and the fast writes of NAND, PCM has the ability to address the entire



memory market and be a key driver for future growth over the next decade.

Alverstone is a 128Mb device built on 90nm and is intended to allow memory customers to evaluate PCM features, allowing cellular and embedded customers to learn more about PCM and how it can be incorporated into their future system designs.

Source: Intel

Citation: Intel, STMicroelectronics Deliver Industry's First Phase Change Memory Prototypes (2008, February 6) retrieved 28 April 2024 from <u>https://phys.org/news/2008-02-intel-stmicroelectronics-industry-phase-memory.html</u>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.