

AMD, Partners Produce Test Chip Using EUV Lithography

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AMD, working together with its research partner, IBM, announced it has produced a working test chip utilizing Extreme Ultra-Violet (EUV) lithography for the critical first layer of metal connections across the entire chip.

Previous projects utilizing EUV to produce working chip components were only “narrow field”, covering just a very small portion of the design. The work of AMD, IBM, and their partners at the UAlbany NanoCollege’s Albany NanoTech Complex, will be presented by Dr. Bruno La Fontaine of AMD at the premier lithography conference in the industry on Tuesday. The paper will show successful integration of “full-field” EUV lithography into the fabrication process across an entire 22 mm x 33 mm AMD 45 nm node test chip.

“This important demonstration of EUV lithography’s potential to be used in semiconductor manufacturing in the coming years is encouraging to all of us in the industry that benefit from chip feature sizes shrinking over time,” said La Fontaine. “Although there is still a lot of work to be done before the industry can use EUV lithography in high volume production, AMD has shown it can be integrated successfully in a semiconductor fabrication flow to produce the first layer of metal interconnects across a full chip.”

“Collaborative research is essential to enabling advancements in semiconductor research,” said David Medeiros, manager of Patterning Research for IBM in Albany, NY. “Our partnerships at the Albany

facility are allowing for assessment of the various aspects of the EUV infrastructure in an integrated way, and will be the true test of this technology's readiness for manufacturing.”

Lithography is how highly complex chip designs with millions of transistors, like microprocessors, are transferred onto the silicon wafer for the many layers required to build a chip. As chip designers continue to add functions and increase the performance of their products, making the transistors smaller and smaller makes more transistors available within a given area. How small transistors and the metal lines that connect them can be made is directly related to the wavelength of light that is used to project a chip design onto a wafer. EUV lithography uses a wavelength of 13.5 nm, significantly shorter than today's 193 nm lithography techniques, allowing the traditional scaling of chip feature sizes to continue.

The AMD test chip first went through processing at AMD's Fab 36 in Dresden, Germany, using 193 nm immersion lithography, the most advanced lithography tools in high volume production today. The test chip wafers were then shipped to IBM's Research Facility at the College of Nanoscale Science and Engineering (CNSE) in Albany, New York where AMD, IBM and their partners used an ASML EUV lithography scanner installed in Albany through a partnership with ASML, IBM and CNSE, to pattern the first layer of metal interconnects between the transistors built in Germany.

After patterning, etch and metal deposition processes, among others, the EUV device structures underwent electrical testing at AMD, with transistors showing characteristics very consistent with those of test chips built using only 193 nm immersion lithography. These wafers will receive additional metal interconnect layers using standard Fab processing so that large memory arrays can also be tested.

The next step in proving viability of the EUV lithography for production will be to apply it not only to metal interconnects but to all critical layers to show an entire working microprocessor can be made utilizing EUV lithography. EUV lithography will need to be fully qualified for production prior to 2016, when the 22 nm half-pitch node on the International Technology Roadmap for Semiconductors is expected to be reached.

Source: AMD

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