

Toshiba develops basic technology for world's smallest flash memory element in 10nm generation

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Toshiba Corporation today announced that it has developed a new double tunneling layer technology applicable to future 10nm generation flash memories.

This elemental technology opens the way for memory devices with densities of over 100 gigabits in the 10nm generation, which lies four generations ahead. The technology was today announced at the IEDM (International Electron Devices Meeting) held at Washington D.C., U.S.A.

Toshiba developed a tunnel layer, which controls in and out of electron, in the SONOS (Silicon Oxide Nitride Oxide Semiconductor) type device structure, a memory structure that holds electrons in the nitride layer in the gate insulator.

The new structure sandwiches a 1.2 nm silicon nanocrystals layer between the 1nm thickness oxide films, achieving long-time data retention and high speed writing and data deletion at the same time, using the natural characteristic that resistance changes with changes in gate voltage. As the new tunnel layers are thinner than early version SONOS element tunnel layers, it is easier to migrate to advanced devices with finer lithography.

Toshiba also increased the saved electrons amount by changing the



nitride film from Si_3N_4 to Si_9N_{10} , a material that contains more silicon, and optimized such aspects of the element structure as channel impurity concentration. The prototype has realized and maintained equivalent to over 10 years performance.

Toshiba is investigating various technologies for future advanced memories, including 3D structures, and believes that realizing operation in the 10nm generation with its new double tunneling layer technology is a step forward to future practical devices.

Source: Toshiba

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