Pushing the limits of chip miniaturisation

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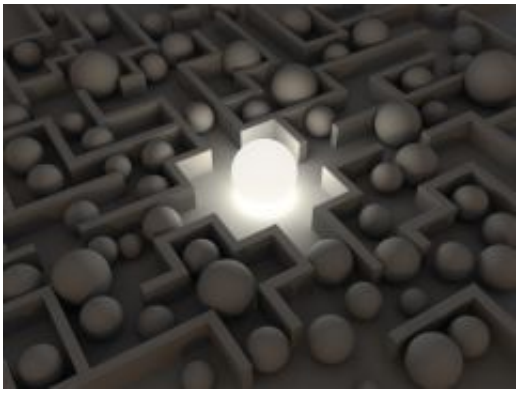

Over the last four decades, computer chips have found their way into virtually every electronic device in the world. During that time they have become smaller, cheaper and more powerful, but, for a team of European researchers, there is still plenty of scope to push back the limits of miniaturisation.

The first generation of CMOS (complementary metal-oxide semiconductor) chips were based on a design process with lithographic features defining regions inside the transistors of 10 micrometres or more. The chips in most products in use today have features more than a hundred times smaller – just 65 nanometres (nm) or 90nm, approximately 1,000 times less than the width of a human hair. That may be small, but in the competitive semiconductor industry, where size is of high importance, it is not small enough.

A reduction in minimum feature size means more transistors per chip, more transistors means more computing power, and more power means electronic systems – mobile phones, PCs, satellites, vehicles, etc. – will gain in functionality and performance. And, because the processed silicon wafers out of which chips are made are expensive (setting up a factory to produce them costs €3 billion) using less of them to do more means the trend toward such devices becoming cheaper can continue.

“The semiconductor industry is in the business of selling square millimetres of silicon. So, by cramming more transistors into a chip you’re delivering more capacity, more functionality and more computing power for the same price. It’s why things like mobile phones, LCD TVs and DVD players are coming down in price,” notes Gilles Thomas, the director of R&D Cooperative Programs at STMicroelectronics in Crolles, France, the world’s fifth biggest semiconductor manufacturer and Europe’s largest semiconductor supplier.

Taking the 'O' out of CMOS

Over the last three and a half years, STMicroelectronics has coordinated two large EU-funded projects to push back the limits of miniaturisation in the semiconductor industry. The NanoCMOS initiative, ending in June 2006, developed the technology to create a 45nm generation (or technology node) of chips.

A follow-up project, called Pullnano and coordinated by Thomas, is currently working on developing nodes as small as 32nm and even 22nm. At that diminutive size, semiconductor manufacturing is continuing to test Moore’s Law, an assumption spelled out by Intel co-founder Gordon E Moore, in 1965, predicting that the number of transistors that can be cost-effectively placed on a chip will double approximately every two years.

“The work of NanoCMOS and Pullnano has moved in that direction, although there is probably 12 or 15 more years to go before we hit a practical and economical limit on how small the nodes can become,” Thomas explains.

At the 32nm scale, in particular, quantum mechanical effects come into play in a big way. One major problem the Pullnano researchers have solved is reducing current leakage at the logic gate by using a hafnium compound-based insulator with higher dielectric strength than traditional silicon dioxide.

“We’ve achieved a 100-fold reduction in gate leakage,” Thomas says, noting that it is the first time the oxide – the ’O’ in CMOS – has been replaced with a different material.

Semiconductor makers’ “million-dollar question”

But as nodes keep getting smaller, a point will inevitably be reached when it is simply no longer feasible to continue to reduce the minimum feature size to make space for more transistors. Thomas describes this point as the semiconductor industry’s “million-dollar question”, although he estimates that it will probably be around the 16nm or 11nm mark.

“At that point it would not be economical or practical to go smaller, even though, in theory, it would be possible,” he says.

Even so, there is still some time before that point is reached. STMicroelectronics is due to start sampling the 45nm node semiconductors that the NanoCMOS project helped develop from next year, with a view to placing electronic systems using them in consumers’ hands by 2009.

By 2011, the Switzerland-headquartered company expects to start

commercialising the 32nm node semiconductors being developed in the Pullnano initiative, with a view to developing a commercially viable 22nm process a couple of years after that.

“The 45nm process has already been validated through the production of an SRAM [static random access memory] chip, which we use to benchmark the performance of each generation. We will do the same with the 32nm process,” Thomas says.

NanoCMOS, which involved 20 partners, and Pullnano, which involves 38 partners, have helped give Europe an edge in semiconductor manufacturing, suggests Thomas, although he notes that the highly competitive sector remains dominated by American and Asian giants such as Intel and Samsung. Nonetheless, there is plenty of room for future growth, even as chips become cheaper.

Consumers will be the biggest beneficiary of the continuation of this miniaturisation trend. The economies of scale created within the $260 billion (+/- €183 billion) semiconductor industry have put electronics within the reach of the masses as the cost per transistor has fallen 2,500 times over the last 25 years. This is thanks to shrinking feature sizes and to increases in transistor manufacturing capacity by a factor of some 30,000.

“Just look at computer memory, in the early 1970s one megabyte cost more than a house, now it costs less than a piece of candy,” Thomas notes.

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