Tunneling Electrons Do Math

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Using a novel computing paradigm involving counting single electrons, computer engineers have designed nano-sized circuitry that allows tunneling electrons to perform mathematical division calculations.

While other methods utilizing quantum mechanical behavior have been proposed to increase computing power, these technqiues have yet to take full advantage of quantum mechanical properties on the nanoscale—namely, high speed and low power consumption.

Cor Meenderinck, a PhD student in Computer Engineering, and Sorin Cotofana, an Associate Professor in Computer Engineering, from the Delft University of Technology in the Netherlands, have recently published their research on a quantum mechanical behavior called single-electron tunneling (SET) in *IEEE Transactions on Nanotechnology*. Building on their past SET paradigms that perform addition and multiplication operations, Meenderinck and Cotofana have presented three schemes that use tunneling electrons to quickly divide.

Electron tunneling is a phenomenon on the quantum scale that enables single electrons to "jump" across forbidden energy states due to their wave-like properties. A few scientists have recently been experimenting with SET circuits based on tunnel junctions that consist of a thin insulating material layered between conducting material. Although charge transport across an insulator is prohibited in classical mechanics, electrons can tunnel one at a time through an ultrathin insulator in quantum mechanics. Electrons can represent bits, making SET a potential candidate to succeed CMOS technology.

"As far as we know, very few people have been designing circuits with SET and we are not aware of any division implementations," Cotofana told *PhysOrg.com*. "Thus comparison is limited to CMOS. Our circuits basically compute analog values. However, due to the discreteness of electrons (if the circuit is designed properly, an electron tunnels or not and electrons are localized on either side of the junction) we end up with digitized values; that is, the number of electrons present in a reservoir is the represented value."

Meenderinck's and Cotofana's first SET design to perform division was based on a sequential approximation of the quotient. The scheme uses electron counting, with three charge reservoirs that store electrons for the dividend Z, quotient Q, and product of Q and the divisor D (Q x D).

In brief, here's how it works: The value of charge reservoir Q is reset to zero before each computation, and electrons tunnel from Q to reservoir Q x D, one at a time, until the value of reservoir Q x D equals that of reservoir Z. The final answer to the problem is the value of reservoir Q; since removing electrons increases the value of the reservoir, this is a positive value.

The researchers improved this simple but limited design by transferring electrons in groups using a "building blocks" method, which decreased unwanted delay and could calculate a remainder. In reservoir Q, electrons are grouped in blocks in logarithmic numbers (e.g. in groups of 1, 2, 4, 8, etc.). An electron block estimates if its transfer would cause the value of reservoir Q x D to exceed that of reservoir Z. If so, the electron block is not transferred, and the next smaller electron block evaluates the same condition.

For example, for 22 divided by 4, one block of 4 electrons, zero blocks of 2 electrons, and one block of 1 electron are transferred to create a positive charge of 5 in reservoir Q. The remainder is calculated with a

subtraction block, which evaluates the difference between the values of reservoirs Z and Q x D (in this case, 22-20=2).

The researchers' third scheme is fine-tuned further, and is based on the computation of periodic symmetric functions (PSF). A PSF block based on an electron trap has a periodic transfer function, of which the period can be dynamically adjusted by using a voltage controlled capacitor. A device called a varactor would be used in place of a capacitor, which is currently still theoretical for the nanoscale.

The PSF scheme resulted in the best performance out of the three schemes, with a worst-case delay of 18 ns and a worst-case energy consumption of 2.3 eV. Meenderinck explained that an accurate comparison to CMOS is difficult, but to give an idea of the difference, he looked at a recent publication on CMOS dividers ('Low Power Self-Timed Radix-2 Division,' Jae-Hee Won and Kiyoung Choi, *ISLPED*, 2000).

"We calculated a delay of 18 ns and an energy consumption of 3.7e-19 J," he said. "The scheme of Won and Choi has a delay of 33.8 ns and an energy consumption of 3.4e-9 J. Clearly, the energy consumption is the key benefit of our SET circuit. Considering that power has become one of the main design constraints, SET becomes a serious candidate for the post-CMOS era."

Meenderinck also added that, although the latency of the two circuits does not appear to differ much, that number could change when using alternative equations.

"We used the equations of the orthodox theory, which is generally accepted by the research community in the field," he said. "However, there are some researchers (mainly from the circuit theory area) that disagree with this theory. For example, J. Hoekstra proposed a circuit

theory ('On the impulse circuit model for the single-electron tunnelling junction,' *International Journal of Circuit Theory and Applications*, 2004) in which the delay is calculated as the RC product of the circuit. Using this theory, the delay we report would be much smaller—reduced by a factor of 100 or more."

For engineers who use SET to look beyond traditional ways of computation, Meenderinck and Cotofana predict that the technique has the potential to make many such improvements in future computing.

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