MIT team aims to optimize chip designs

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Computer chips inside high-speed communication devices have become so small that tiny variations which occur during chip fabrication can make a big difference in performance.

The variations can cause fluctuations in circuit speed and power causing the chips not to meet their original design specifications, says MIT Professor Duane Boning, whose research team is working to predict the variation in circuit performance and maximize the number of chips working within the specifications.

The researchers recently developed a model to characterize the variation in one type of chip. The model could be used to estimate the ability to manufacture a circuit early in the development stages, helping to optimize chip designs and reduce costs.

"We're getting closer and closer to some of the limits on chip size, and variations are increasing in importance," says Boning, a professor of electrical engineering and computer science (EECS) and associate head of the department. "It's becoming much more difficult to reduce variation in the manufacturing process, so we need to be able to deal with variation and compensate for it or correct it in the design."

Boning and EECS graduate student Daihyun Lim's model characterizes variation in radio frequency integrated circuits (RFICs).

RFIC chips are integral to many of today's high-speed communication and imaging devices, such as high-definition TV receivers. Shrinking the

size of a chip's transistors to extremely small dimensions (65 nanometers, or billionths of a meter), improves the speed and power consumption of the RFIC chips, but the small size also makes them more sensitive to small and inevitable variations produced during manufacturing.

"The extremely high speeds of these circuits make them very sensitive to both device and interconnect parameters," said Boning, who is also affiliated with MIT's Microsystems Technology Laboratories. "The circuit may still work, but with the nanometer-scale deviations in geometry, capacitance or other material properties of the interconnect, these carefully tuned circuits don't operate together at the speed they're supposed to achieve."

Every step of chip manufacturing can be a source of variation in performance, said Lim. One source that has become more pronounced as chips have shrunk is the length of transistor channels, which are imprinted on chips using lithography.

"Lithography of very small devices has its optical limitation in terms of resolution, so the variation of transistor channel length is inevitable in nano-scale lithography," said Lim.

The researchers' model looks at how variation affects three different properties of circuits-capacitance, resistance and transistor turn-on voltage. Those variations cannot be measured directly, so Lim took an indirect approach: He measured the speed of the chip's circuits under different amounts of applied current and then used a mathematical model to estimate the electrical parameters of the circuits.

The researchers found correlations between some of the variations in each of the three properties, but not in others. For example, when capacitance was high, resistance was low. However, the transistor

threshold voltage was nearly independent of the parasitic capacitance and resistance. The different degrees of correlation should be considered in the statistical simulation of the circuit performance during design for more accurate prediction of manufacturing yield, said Lim.

The researchers published their results in two papers in February and June. They also presented a paper on the modeling of variation in integrated circuits at this year's International Symposium on Quality Electronic Design.

Source: MIT