UMC, ARM Partner to Deliver Comprehensive SOI Solutions for 65nm Technology

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UMC and ARM today announced that a test chip built with ARM SOI (Silicon On Insulator) libraries was taped-out successfully on UMC's 65-nanometer (nm) SOI process. The test chip consists of a set of ARM physical IP that uses a standard cell library, an I/O library and a single-port SRAM memory compiler. This tape-out at UMC represents the next step towards mainstream adoption of nanometer SOI technology for improved speed and power in complex system on chips (SOCs).

Semico Research recognizes semiconductor chip performance is increasingly pushing the limits of bulk CMOS. "High-performance chips offer the best near-term opportunities for SOI. Portable products are rapidly evolving into high-performance audio and video platforms that can utilize the speed and power advantages offered by SOI technology. Likewise, high-performance computing, communications and network applications are ripe for SOI technology in the next few years," said Jim Feldhan, president of Semico Research. "Semico believes companies that invest in SOI at 65 and 45nm will be best positioned for market opportunities at 32nm. ARM and UMC's venture into SOI is a significant step. It represents the first strong commitment of a Taiwanese-based foundry to SOI technology and will provide fabless and IDM companies additional market choices."

While UMC has been developing SOI technology for many years, this particular advance began in January 2006, when UMC started a strategic

partnership with Soisic. ARM has continued this partnership, after acquiring Soisic and partnering with Soitec in October 2006, and has begun to offer SOI libraries alongside its full range of physical IP for bulk CMOS processes. To help UMC derive an SOI version of its existing bulk 65nm CMOS L65SP, ARM provided the specific modules required to develop and qualify the process, including design rules, electrical characterization of the devices and modeling for circuit simulation. The resulting L65SOI process features nominal 1V multi-threshold voltage thin gate oxide transistors, nominal 2.5V thick gate oxide transistors for I/O and a nominal 1V 0.62 square-micron 6-transistors SRAM bitcell. A full process design kit is now in place and ready for use by customers.

"We are very happy with the result of this partnership, which has allowed us to become the first foundry to develop and offer a complete 65nm SOI solution," stated Lee Chung, vice president of Corporate Marketing at UMC. "We leveraged ARM's strong SOI expertise from the design support side along with our volume production 65nm process to quickly develop and bring this SOI process to the market. We look forward to offering this competitive technology to our foundry customers."

The ARM standard cells used in the test chip support multi-VT and multi-power supply circuit designs, the I/O is 3.3V signal tolerant and the memory compiler is optimized for high-speed and low-power consumption. Initial circuit analysis indicates that the design saves up to 20 percent in area and 30 percent in power consumption, compared to a part produced to reach the same performance on bulk CMOS at 65nm. SOI technology also offers up to 28 percent speed boost with 10 percent power reduction over bulk CMOS.

"Strong demand from IDMs for the performance provided by SOI technology exists in the market today," said Tom Lantzsch, vice

president, Marketing, Physical IP, ARM. "We anticipate that this new process, available through UMC, will enable leading fabless design companies to assess SOI technology and begin pilot projects. The next step will be to broaden the offerings, extend to more advanced process nodes and introduce a full foundry program similar to our offerings in the bulk CMOS space."

Source: UMC

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