

Algorithm could help chipmakers work with tangles of nanotubes

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Concerned that current methods for making computer chips might become stymied as components keep shrinking, many engineers are looking for circuit building blocks with improved electrical properties.

Among the most promising are stringy carbon nanotubes that capably form transistors to switch current on and off. But the nanotubes tend to grow with unpredictable kinks and bends that could cause bad wiring connections. This week at the Design Automation Conference in San Diego, a group of Stanford engineers will present a way to design circuits that should work even when many of the nanotubes in them are twisted and misaligned.

"The question is what's next in chip technologies," says Subhasish Mitra, an assistant professor of electrical engineering and computer science. "That's why nanotechnology is important. But you want to make sure that you are not in a lab making something that chip designers cannot actually use."

To prevent that, he and electrical engineering Professor H.-S. Philip Wong, working with chemistry Professor Chongwu Zhou at the University of Southern California, have been looking closely at how nanotubes end up resting on the surfaces of experimental chips.

"It's not as bad as a plate of noodles," Mitra says. "You want to create transistors out of these things, and hook up these transistors and make them turn on and off independently. But if twisted carbon nanotubes, for

example, short out the circuit, you lose the opportunity to do that."

Making messy workable

What Mitra, Wong and graduate students Nishant Patil and Jie Deng have realized is that if nanotubes are always going to be somewhat askew, engineers will have to design circuits that can work regardless of where and how the tubes lie. They started by coming up with a single circuit element, a NAND gate, that was immune from the vagaries of its underlying nanotube layout.

From that single element that could function despite misalignments, they abstracted and generalized the math to come up with an algorithm that can guarantee a working design for any circuit element, Mitra says, even when a large number of nanotubes are misaligned.

Using simulations developed by Wong and Deng, the group has been able to show that not only do the algorithm's designs work, but they also don't appear to exact a significant financial, speed or energy price compared to traditional designs, Mitra says.

The key to determining whether a circuit element is immune to nanotube misalignment is breaking up each circuit element into a fine grid that can be analyzed mathematically. Doing this in the abstract with models allows engineers to determine which grid squares nanotubes must pass through and which they shouldn't traverse to make a design work correctly. To eliminate unwanted connections, nanotubes in so-called "illegal" regions can then be either chemically etched away or rendered electrically irrelevant in other ways.

The Stanford algorithm takes this all several steps further, applying sophisticated mathematics to automatically determine where the legal and illegal regions should be in the design of a circuit element with a

particular function.

"You not only determine whether something is immune or not, but can automatically generate circuit designs that are guaranteed to be immune," Mitra says.

While the algorithm can overcome all the bad connections that errant nanotubes make, it cannot guarantee that a nanotube will always make a desired connection. Nanotubes also have other problems that remain unsolved, Mitra points out. Some, for example, always conduct electricity instead of switching on and off like a semiconductor should.

The group's next step is to move beyond simulation to build and test real circuit elements according to the algorithm's output. While more work is necessary to deliver the promise of nanotube technology, solving the misalignment problem would be a significant step.

"Carbon nanotube transistors show great promise as extensions to silicon transistors due to their fast speed, small size and lower energy consumption," Patil says. "Using this technique, we can make larger and more complex circuit blocks with them."

Wong speculates that the advance could eventually spill over from chips to assist engineers facing analogous challenges.

"A similar methodology can be applied to many emerging technologies," he says. "The concept of not having to define everything with high precision is germane to engineering robust systems."

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