Solutions Emerging for Wafer Cleaning at 45 nm and Beyond

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Potential solutions are starting to emerge for preparing wafers for manufacturing at and beyond the 45 nm technology generation, technologists indicated at a recent industry meeting organized by SEMATECH.

The 2007 Surface Preparation and Cleaning Conference, held here in late April, reported several techniques for non-damaging particle removal from wafer surfaces, along with multiple methods for removing photoresist with minimal silicon and oxide loss.

These and other conference presentations were aimed at acquainting equipment companies and chip-makers with the latest innovations in wafer and mask-cleaning technologies, in an effort to surmount the related challenges posed at 45 nm (and for subsequent generations for some advanced manufacturers) by the *International Technology Roadmap for Semiconductors* (ITRS).

“The 45 nm generation is coming up fast – and some chip-makers are there already – and many of the manufacturing issues are connected to surface preparation and cleaning,” said SEMATECH’s Joel Barnett, conference chair. “The conference made it clear that many of our chemistries and approaches will have to change, but that plenty of potential solutions are being considered for 45 nm and beyond.”

For example, 12 presentations were offered on non-damaging nanoparticle removal, including:

-- Shock tube-enhanced laser-induced plasma (LIP) shockwaves for sub-50 nm nanoparticle removal, from Clarkson University. This approach confines LIP beams to specially engineered “shock tubes” to increase the cleaning power of shock waves.

-- Plasma-assisted cleaning by electrostatics (PACE), offered by the University of Illinois at Urbana-Champaign. This technology utilizes broad-area plasma to provide a negative charge to contamination, allowing it to be repelled electrostatically.

-- An ionized molecular-activated coherent solution, proposed by Nano Green Technology, Inc. This method uses a charged solution of ammonia in water to form clusters that attract particles at the molecular level, without damaging the wafer surface.

-- Parametric nanoscale cleaning from Lancetta, Inc., which suggested a technology that removes particles by forming nanoscale bubbles to absorb the contaminants.

On photoresist issues, seven papers offered new or enhanced methods for minimizing silicon and oxide loss during removal. These included photoreactive cleaning from UVTech Systems; a CO_2 cryogenic press and non-oxidizing chemistry from DuPont Electronic Technologies, EKC Technology, and BOC Eco-Snow Systems; and methodologies for all-wet chemistries from FSI International and SEZ Group.

Earlier in the conference, keynote speaker Jadgish Prasad of AMI Semiconductor urged engineers to consider the requirements of surface cleaning when designing future generations of microchip circuits. Design dominates how wet processing is done, and processing limitations in turn influence the design process, he said.

Reflecting a chip-maker’s perspective, Prasad emphasized the critical

influence of surface preparation on yield and reliability. “Sixty percent of fab-related (yield) problems are related to cleans, and another 12 percent to etching steps,” he said. Prasaid predicted that manufacturers will need to adopt new etch chemistries and cleaning regimens for the 45 nm generation and beyond.

High-k materials and metals gates also are slated for introduction at 45 nm. Although this year’s conference did not address these approaches, SEMATECH has published numerous papers detailing high-k related surface preparation processes and continues to develop processes related to dual metal gate and higher-k gate processes.

Capping the meeting was a panel of industry experts who analyzed the key challenges of surface preparation at 45 nm. Their comments, captured in a webcast by Semiconductor International, pointed to the need for significantly different technologies in the field.

“Our purpose in offering the conference is to help prepare our audience for the cleaning demands of 45 nm technology,” Barnett said. “Our speakers gave them plenty of leading-edge data to meet that test.”

Source: SEMATECH