

Intel Aims High at IDF

April 17 2007

On the first day of the Intel Developer Forum, the company details several new products on its road map, including its 45-nm "Penryn" processors and its new System on a Chip technology. Intel is working to show that there is more to chip design than clock speed.

At its spring Developer Forum, which kicked off on April 17 in Beijing, Intel executives <u>detailed several new developments</u> on the company's road map, including new performance numbers for its line of "Penryn" 45-nanometer processors and details about its SOC (System on a Chip) microarchitecture.

The microprocessor announcements at the conference seem to show an emphasis on the multifaceted possibilities of what Intel can accomplish beyond increasing clock speed and performance.

For example, Intel announced that it will start producing a family of processors called "Tolapai" that will use the new SOC microarchitecture. The new architecture, according to Intel, will combine IA (Intel Architecture) x86 processor cores on the same piece of silicon as the I/O and memory control hub.

Intel, based in Santa Clara, Calif., had already announced that its embedded chip road map would include processors that use SOC microarchitecture. In addition, for use within the enterprise space, Intel executives said they plan to detail how the SOC technology will work with a series of consumer-based gadgets, including set-top boxes and multimedia players.



The Tolapai microprocessors will include a new accelerator technology called QuickAssist. Much like a similar program from Advanced Micro Devices called Torrenza, QuickAssist will allow third-party accelerators to work with IA microprocessors.

Intel officials are also expected to announce that the company is working on developing products that use a new IA microarchitecture called "Larrabee." While Intel has not divulged many details of this long-rumored architecture, this technology builds on an announcement earlier in 2007 that it had developed an experimental microprocessor capable of delivering teraflops - trillions of calculation per second - of performance.

With the Larrabee architecture, Intel is proposing to develop a new generation of x86 IA architecture that can scale upward, offering microprocessors that can perform trillions of calculations per second. Executives said this type of technology will find a home in a number of enterprise-class products, including scientific computing, financial analytics and health applications.

In addition to detailing future developments, Intel also plans to demonstrate the performance of its Penryn family of processors. The first of these processors are due later in 2007.

On March 28, the company offered additional details of its 45-nanometer processors, which use the company's High-k processor technology.

At the April 17 conference in Beijing, company officials went a step further and disclosed new performance specifications. For example, a Penryn processor with a 1600MHz FSB (front side bus) in a workstation or Penryn processor with a 1300MHz FSB in a server will offer 45 percent better performance for bandwidth-intensive applications and 25



percent greater performance for a server using Java. In this scenario, Intel compared the two pre-production processors with a quad-core Xeon 5355 processor.

Intel also compared a Penryn processor with a clock speed of 3.3GHz, a 1333MHz FSB and 12MB of Level 2 cache with its quad-core Core 2 Extreme QX6800, which the company just released on April 9. The results showed a 25 percent greater performance with three-dimensional rendering, a 40 percent increase in gaming performance and a 40 percent increase in video encoding.

Finally, Intel executives also offered details about some of its enterprise technologies that it had been discussing in the weeks leading up to the opening of its Developer Forum.

Intel's "Caneland," a new Xeon MP platform due in the third quarter of 2007, will be offered as the Xeon 7300 processor series and will come in 80- and 50-watt versions for blade servers. Hewlett-Packard on April 17 also announced that it would be one of the first OEMs to offer these processors, which have been code-named Tigerton, in its systems.

Intel also detailed its plans to roll out its next generation of vPro technology, called "Weybridge," in the second half of this year. On April 4, the company announced that it would offer vPro in its upcoming Centrino platform.

The Weybridge platform will also use a new Intel 3-Series chip set, called "Bear Lake."

Copyright 2007 by Ziff Davis Media, Distributed by United Press International



Citation: Intel Aims High at IDF (2007, April 17) retrieved 19 April 2024 from https://phys.org/news/2007-04-intel-aims-high-idf.html

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.