Monarch system-on-a-chip excels in early testing

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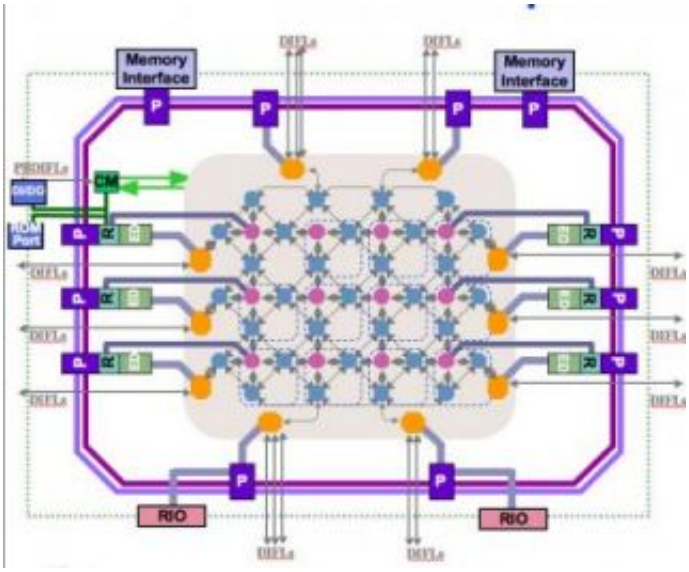
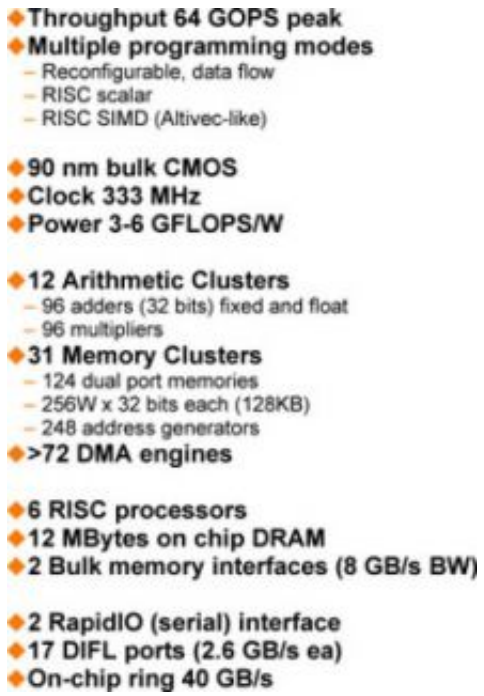


MONARCH system changes to address different computing challenges. Credit: USC Information Sciences Institute

A revolutionary processor package that changes its architecture to adapt to the demands of different computing tasks more than met design expectations in recent trials.

Near-term applications for the MONARCH (Morphable Networked Micro-Architecture) system designed by the USC Information Sciences Institute and Raytheon include space radar and video processing, which require small size and low power.

Raytheon also is investigating high-end commercial applications such as use in smart cars and highways and in medical imaging, as well as exploring a method for countering GPS jamming for the military.



Technical specifications of MONARCH system. Credit: USC Information Sciences Institute

During Phases I and II of the program, an ISI group headed by John Granacki developed the MONARCH architecture, working with the Advanced Concepts and Technology group of Raytheon Space and Airborne Systems on a contract from DARPA.

Granacki is director of the Advanced Systems Division at ISI, and Research Associate Professor of Electrical Engineering Systems and Biomedical Engineering in the USC Viterbi School of Engineering.

"What we have been creating is essentially a supercomputer on a chip," he said, "and not just a supercomputer, but a flexible supercomputer reconfigures itself into the optimal supercomputer for each specific part of a multi-part task."

This flexibility means MONARCH allows a significant reduction of the amount of hardware (and therefore power) required for computing systems, while still achieving extremely high (teraflop) throughput. Because of the memory integrated on the chip, very small systems may be implemented with only a single MONARCH device.

For larger implementations, hardware demand is further reduced by MONARCH's ability to "morph" devices to so they can perform downstream tasks instead of sitting idle while waiting for fresh input

The MONARCH chip may also serve as a system building block, allowing systems of different sizes to be based on arrays of devices. Each device has input/output ports to enable seamless data movement among multiple chips. The device has two off-chip memory interfaces for large problems. Finally, every chip is equipped with two RapidIO interfaces for connecting to industry-standard equipment.

According to Granacki, MONARCH's polymorphic capability and super efficiency enable the development of DoD systems that need very small size, low power, and in some cases (particularly systems to be used in space) radiation tolerance.

"Typically, a chip is optimally designed either for front-end signal processing or back-end control and data processing," explained Nick Uros, vice president for the Advanced Concepts and Technology group of Raytheon Space and Airborne Systems.

"The MONARCH micro-architecture is unique in its ability to

reconfigure itself to optimize processing on the fly. MONARCH provides exceptional compute capacity and highly flexible data bandwidth capability with beyond state-of-the- art power efficiency, and it's fully programmable."

In preliminary tests in the Phase III evaluation, a prototype system consisting of just one of the new devices, provided sustained throughput of 64 gigaflops (floating point operations per second) with more than 60 gigabytes per second of memory bandwidth and more than 43 gigabytes per second of off-chip data bandwidth.

In addition to the ability to adapt its architecture for a particular objective, the MONARCH computer is also believed to be the most power- efficient processor available. "MONARCH outperformed the Intel quad-core Xeon chip by a factor of 10," said Michael Vahey, Raytheon's principal investigator for the company's MONARCH technology.

Source: University of Southern California