Hybrid nano-CMOS chips could be far denser, but cooler

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Hewlett-Packard today announced research that could lead to the creation of field programmable gate arrays (FPGAs) up to eight times denser – while using less energy for a given computation – than those currently being produced.

Moreover, such chips could be built using the same sized transistors as those used in today's FPGA design, meaning they could be built in current fabrication facilities with only minor modifications.

FPGAs are integrated circuits with programmable logic components and interconnects that can be adapted by end-users for specific applications. They are used in a wide range of industries, including communications, automotive and consumer electronics.

The technology calls for a nanoscale crossbar switch structure to be layered on top of conventional CMOS (complementary metal oxide silicon), using an architecture HP Labs researchers have named "field programmable nanowire interconnect (FPNI)" – a variation on the well-established FPGA technology.

The research, by Greg Snider and Stan Williams of HP Labs, is a featured paper in the Jan. 24 issue of *Nanotechnology*, a publication of the British Institute of Physics ("Nano/CMOS Architectures Using Field-Programmable Nanowire Interconnect"). The research was conducted using classic modeling and simulation techniques, but Williams said HP is working on producing an actual chip using the approach, and could

have a laboratory prototype completed within the year.

“As conventional chip electronics continue to shrink, Moore’s Law is on a collision course with the laws of physics,” said Williams, an HP Senior Fellow and director, Quantum Science Research, HP Labs. “Excessive heating and defective device operation arise at the nanoscale. What we’ve been able to do is combine conventional CMOS technology with nanoscale switching devices in a hybrid circuit to increase effective transistor density, reduce power dissipation, and dramatically improve tolerance to defective devices.”

The work uses a conceptual breakthrough for connecting a crossbar to CMOS by Dmitri Strukov and Konstantin Likharev of Stony Brook University in New York. The HP approach relies on extensive experience in fabricating crossbars and makes a number of changes designed to improve the manufacturability of the circuits.

In the FPNI approach, all logic operations are performed in the CMOS, whereas most of the signal routing in the circuit is handled by a crossbar that sits above the transistor layer. Since conventional FPGAs use 80 to 90 percent of their CMOS for signal routing, the FPNI circuit is much more efficient; the density of transistors actually used for performing logic is much higher and the amount of electrical power required for signal routing is decreased.

The researchers presented a “conservative” chip model using 15-nanometer-wide crossbar wires combined with 45-nm half-pitch CMOS, which they said they believe could be technologically viable by 2010. That would be equivalent to leaping ahead three generations on the International Technology Roadmap for Silicon without having to shrink the transistors, they said.

“The expense of fabricating chips is increasing dramatically with the

demands of increasing manufacturing tolerances," said Snider, senior architect, Quantum Science Research, HP Labs. "We believe this approach could increase the usable device density of FPGAs by a factor of eight, using tolerances that are no greater than those required of today's devices."

Snider and Williams also used a model based on 4.5-nm-wide crossbar wires, which they said could be ready by 2020. The 4.5-nm crossbar architecture combined with 45-nm CMOS would yield a hybrid FPGA about 4 percent the size of a 45-nm CMOS-only FPGA. In this case, the clock speed will likely decrease, but so will energy per computation. The opportunity is in the parallelism offered by FPGAs – with lots of parallelism to exploit, this architecture requires much less energy to operate.

Because of the tiny sizes of the nanowires and switches in the crossbars, the researchers said they expected defect rates to be relatively high. However, with the crossbar interconnect it is possible to route around defects, the researchers said. Their simulations showed that an FPNI chip with 20 percent of the nanowires broken in random locations still had an effective production yield of 75 percent and did not present significant performance compromises, which should make it economically feasible to produce.

Source: Hewlett-Packard